

# I.MX8 DRAM STRESS TEST SUBTESTS OVERVIEW



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# DDR Stress Test

## Overview of DRAM Subtests

- **data is addr test**
  - This test basically programs the source buffer's data words with its address (and immediately read-verifies), then copies (memcpy) the source buffer to a destination buffer and verifies the data transferred correctly.
  - For example, if the source address being written to is "0x80000008", the data value of that address is "0x80000008". Once the source buffer is completely written, the data is transferred to the destination where it is verified.
  - A basic test to ascertain that simple read/writes work
- **row hop read test**
  - This test performs single word reads by hopping from one DRAM row to the next, reading the first column in each row and in each bank. Once all of the rows are read from the first column, the reads start again from the first row, and begin at the second column. The intent is to perform non-sequential reads and to force pre-charge and activate commands before each read access.
- **memcpy SSN armv8 x32 test**
  - This test utilizes a custom written memory copy function that issues load and store pair (LDP, STP) instructions, to test the bursting behavior of the DDR interface. This test uses data patterns to help root out simultaneous switching noise (SSN). This test also breaks up the total DDR density into four "banks" or memory regions, where each bank contains a different SSN data pattern. The test uses various stress patterns such as walking ones and walking zeros, and 0xA's followed by 0x5's.
- **byte-wise SSN armv8 x32 test**
  - The purpose of this test is to root out any SSN within byte lanes. It accomplishes this by writing byte-wise patterns to one location and the inverse of each byte to the subsequent location. Each of the four bytes values are equal to one another and the test increments the byte pattern as follows (with the inverse value in brackets: 0x00000000 [0xFFFFFFFF]; 0x01010101 [0xFEFEFEFE]; 0x02020202 [0xFDFDFDFD]; ... 0xFFFFFFFF [0x00000000]).
- **memcpy pseudo random pattern test**
  - This test utilizes a custom written memory copy function that issues load and store pair instructions to test the bursting behavior of the DDR interface. The data pattern used is pseudo-random. This test also breaks up the total DDR density into four "banks" or memory regions, where each bank contains a different "seed" for each pseudo-random data pattern.
- **IRAM to DDRv2 test**
  - The purpose of this test is to root out any SSN and isolates the DDR read and write accesses by using the Internal RAM (IRAM) as an intermediate data storage location. This test moves data from DDR to IRAM and then from IRAM to a different DDR location, then compares DDR location 1 and location 2. This test is similar to the IRAM\_to\_DDRv1 test (described next), but instead transfers the data 1000 times per test to ensure that the data never changes to root out random glitches. Also, the test uses various data patterns to root out SSN.
- **IRAM to DDRv1 test**
  - The purpose of this test is to root out any SSN and isolates the DDR read and write accesses by using the IRAM as an intermediate data storage location. This test moves data from DDR to IRAM and then from IRAM to a different DDR location, then compares DDR location 1 and location 2.





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