iMX6 TinyRex Baseboard Lite

Variant: Production

23. 10. 2015
V1I1

RELEASED 23-OCT-2015

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

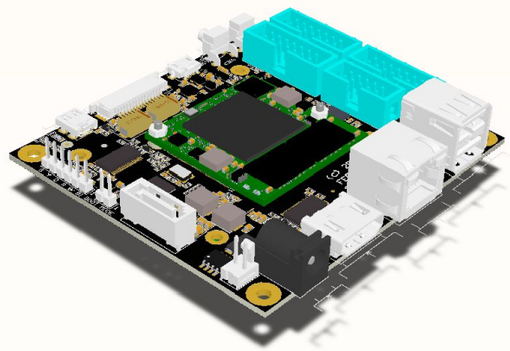
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for debug notes.

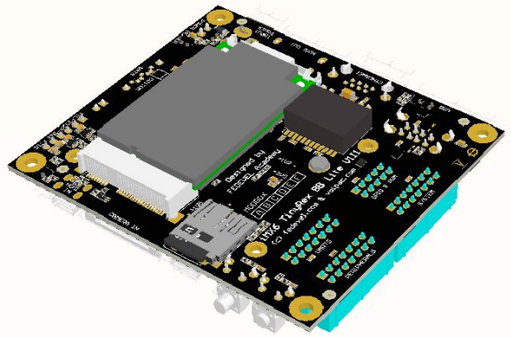
DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

TOP VIEW



BOTTOM VIEW



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iMX6 TinyRex Baseboard Lite

(Block Diagram)

Page 15
Input power Jack (3.2~5.3V DC)

Page 15
Input / Output Power Header (3.2~5.3V DC)

Page 4
Overvoltage Protection

+VIN

HDMI OUTPUT → Page 6 **HDMI (Output)**

VIDEO INPUT (CSI0, parallel camera input, YCbCr 16-bit / 1 cycle)
Digital audio (I2S)
→ Page 4 **HDMI Receiver (ADV7610)**
HDMI INPUT → Page 5 **HDMI Micro (Input)**

CSI (MIPI, differential camera input) → Page 10 **CSI Camera Connector (Raspberry Pi Compatible)**
I2C2, CSI1_PIXCLK, CSI1_GPIO

Page 7 **PCIE Mini**

Page 9 **USB Signal Switch** → Page 9 **USB A Stacked Connector** USB Single (Optional)

Page 9 **USB Signal Switch** → Page 9 **USB0 AB Micro** → Page 9 **+5V USB OTG VBUS Switch** (+5V, +VIN)

Page 10 **SATA Connector**

Page 12 **UART1 Signals Isolation** → Page 12 **UART1 (Debug Console) (FTDI Cable Compatible)**

Page 12 **UART Header (UART2-5)**

Page 11 **Micro SD3 socket (Bootloader + OS) (Push-Push Card Connector)**

Page 13 **SPI Flash**

Page 13 **System Header**

Page 13 **Peripheral Header**

Page 13 **GPIO & PWM Header**

Page 8 **RJ45 1Gb Ethernet**

+3V3 → **USB0 Switch LED** *(GREEN)*
+3V3 → **USB1 Switch LED** *(RED)*
+3V3 → **POWER LED** *(GREEN)*
+3V3 → **USER LED** *(RED)*

RESET Button
User Button

+VIN → Page 14 **DC / DC Boost/Buck Regulator +5V** → +5V
+VIN → Page 14 **DC / DC Boost/Buck Regulator +3.3V** → +3V3
+VIN → Page 14 **DC / DC Regulator +2.5V** → +2V5
+VIN → Page 4 **DC / DC Regulator +1.8V** → +1V8
+VIN → Page 7 **DC / DC Regulator +1.5V** → +1V5

iMX6 TinyRex Module

Page 3 **BOARD CONNECTOR 1**

USER_LED

Page 3 **BOARD CONNECTOR 2**

PCIE
USB1
USB0
SATA
UART1 (RX/TX/RTS/CTS)
UART2, UART4, UART5 (TX/RX)
SYS_POK, SYS_RST, 2xGPIO, 2xPWM
2x I2C (I2C2, I2C3), 1x FLEXCAN
SD card (4 bit SD3)
SPI1 (Bootable)

Page 3 **BOARD CONNECTOR 3 (Optional)**

UART3 (RX/TX/RTS/CTS)
SPI2
CSI1_PIXCLK, CSI1_GPIO
6x GPIO, 2x PWM
Ethernet PHY

UART3 (RX/TX/RTS/CTS)
BUF_SYS_RSTn, RST_BUT
PWR_LED, USR_LED, USR_BUT
I2C1, 2x GPIO, 2x PWM
I2C2, I2C3
SPI2
FLEXCAN1

Page 8 **Magnetics**

http://www.iMX6Rex.com/

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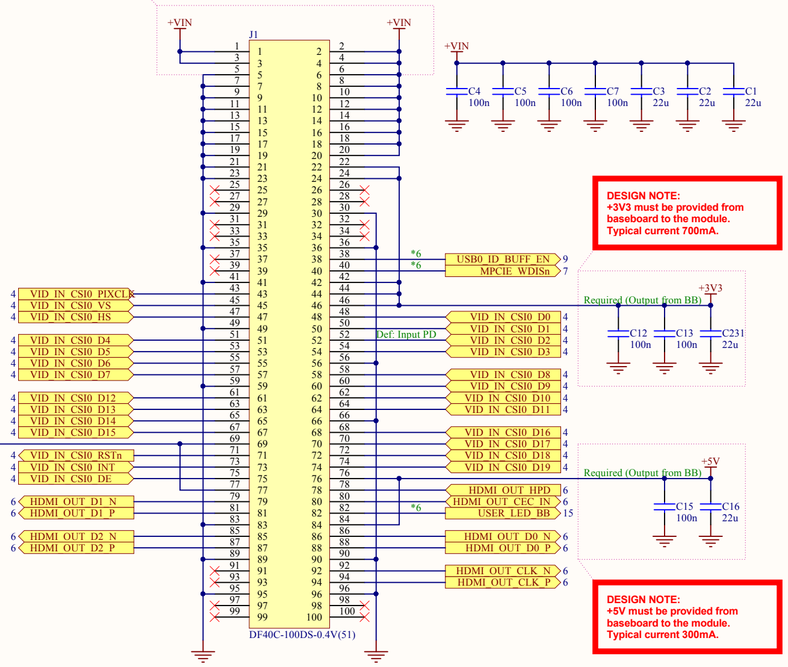
CONNECTORS

DESIGN NOTE:
+VIN must be provided from baseboard to the module.
Maximum current 3.6A.

+VIN = +2.7-5.5 VDC
(Output voltage from BB)



DESIGN NOTE:
+3V3 must be provided from baseboard to the module.
Typical current 700mA.

DESIGN NOTE:
+5V must be provided from baseboard to the module.
Typical current 300mA.

DESIGN NOTE:
*1 Be careful, these pins are connected to +3V0_ALWAYS.

DESIGN NOTE:
*4 These pins have an internal 100k pull down resistor before RESET.

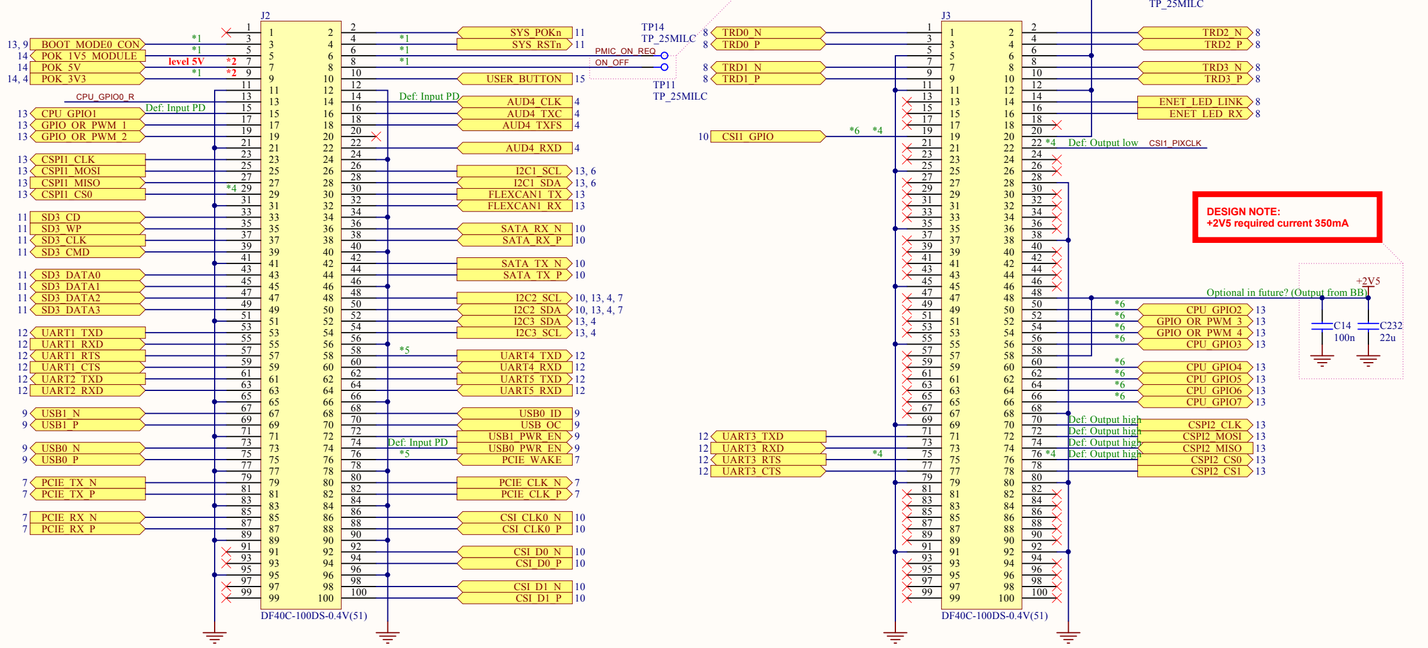
DESIGN NOTE:
*6 These pins use different naming in module and in baseboard schematic. Be sure you set these pins correctly according to the version of the baseboard.

DESIGN NOTE:
***2 This pin must not be left unconnected (See Power Sequencing Page 16).**

DESIGN NOTE:
*5 These pins are set as output with unknown state before the reset. See Table 103 page 167 in IMX6DQAEC.

DESIGN NOTE:
Optional: If ON-OFF operation is required 3V0_ALWAYS source is needed. Testing required.

DESIGN NOTE:
Connector J3 is optional - signals on this connector are not required in the booting process.



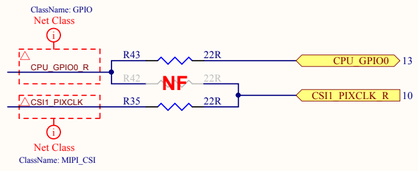
LAYOUT NOTE:
If 1.5mm standoff Board to Board connector is used, do not place any components under the module.

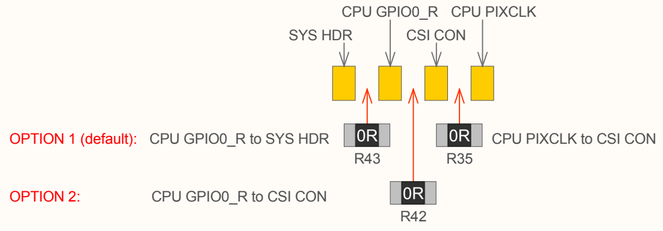
DESIGN NOTE:
Mating connector default: DF40C-100DP-0.4V(51)
http://www.digikey.com/product-detail/en/DF40C-100DP-0.4V%2851%29/H11614TR-ND/1969475

DESIGN NOTE:
Maximum current for the board to board connector is 0.3A per contact.

CPU_GPIO0 & CSI1_PIXCLK Routing

DESIGN NOTE:
Use one of the options to fit series resistors according to the picture below.





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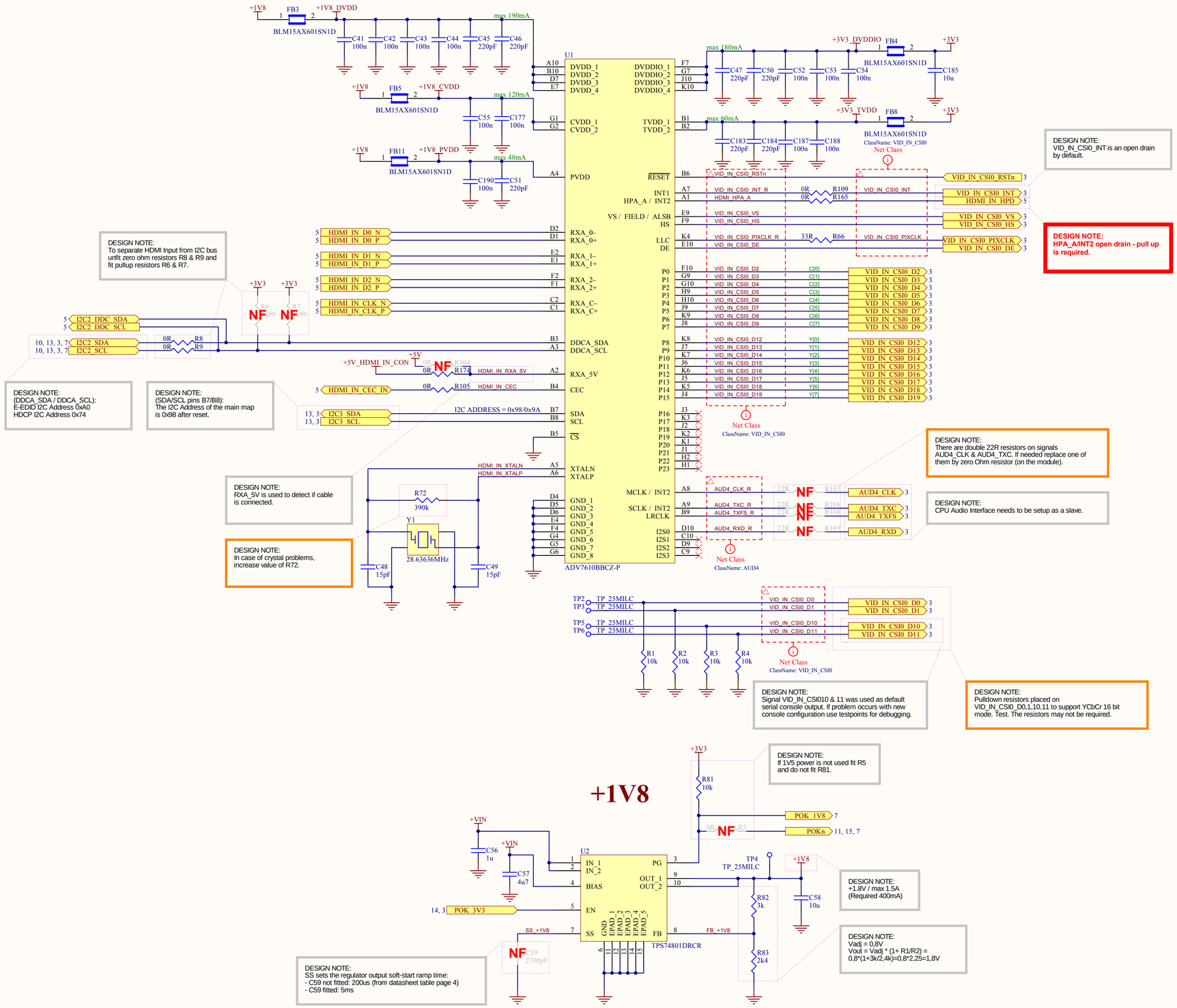
HDMI Video Input



DESIGN NOTE:
iMX6 IPU Sensor Interface Signal Mapping

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 2 cycles	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
IPUx_CSIx_DATA00	—	—	—	—	—	—	—	0	C[0]
IPUx_CSIx_DATA01	—	—	—	—	—	—	—	0	C[1]
IPUx_CSIx_DATA02	—	—	—	—	—	—	—	C[0]	C[2]
IPUx_CSIx_DATA03	—	—	—	—	—	—	—	C[1]	C[3]
IPUx_CSIx_DATA04	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
IPUx_CSIx_DATA05	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
IPUx_CSIx_DATA06	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
IPUx_CSIx_DATA07	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
IPUx_CSIx_DATA08	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
IPUx_CSIx_DATA09	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
IPUx_CSIx_DATA10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
IPUx_CSIx_DATA11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
IPUx_CSIx_DATA12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
IPUx_CSIx_DATA13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
IPUx_CSIx_DATA14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
IPUx_CSIx_DATA15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
IPUx_CSIx_DATA16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
IPUx_CSIx_DATA17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
IPUx_CSIx_DATA18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
IPUx_CSIx_DATA19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

1 IPUx_CSIx stands for IPUx_CSI0 or IPUx_CSI1
2 The MSB bits are duplicated on LSB bits implementing color extension
3 The two MSB bits are duplicated on LSB bits implementing color extension
4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).
5 RGB 16 bits— Supported in two ways: (1) As a "generic data" input, with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.
6 YCbCr 16 bits— Supported as a "generic-data" input, with no on-the-fly processing.
7 YCbCr 16 bits— Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).
8 YCbCr, 20 bits, supported only within the BT.1120 protocol (syncs embedded within the data stream).

DESIGN NOTE:
ADV7610 SDR Output Modes

			SDR 4:2:2		SDR 4:4:4
OP_FORMAT_SEL[7:0]	0x0	0x0A	0x80	0x8A	0x40
Pixel Output	8-Bit SDR ITU-R BT.656 Mode 0	12-Bit SDR ITU-R BT.656 Mode 2	16-Bit SDR ITU-R BT.656 4:2:2 Mode 0	24-Bit SDR ITU-R BT.656 4:2:2 Mode 2	24-Bit SDR 4:4:4 Mode 0
P23	High-Z	Y3, Cb3, Cr3	High-Z	Y3	R7
P22	High-Z	Y2, Cb2, Cr2	High-Z	Y2	R6
P21	High-Z	Y1, Cb1, Cr1	High-Z	Y1	R5
P20	High-Z	Y0, Cb0, Cr0	High-Z	Y0	R4
P19	High-Z	High-Z	High-Z	Cb3, Cr3	R3
P18	High-Z	High-Z	High-Z	Cb2, Cr2	R2
P17	High-Z	High-Z	High-Z	Cb1, Cr1	R1
P16	High-Z	High-Z	High-Z	Cb0, Cr0	R0
P15	Y7, Cb7, Cr7	Y11, Cb11, Cr11	Y7	Y11	G7
P14	Y6, Cb6, Cr6	Y10, Cb10, Cr10	Y6	Y10	G6
P13	Y5, Cb5, Cr5	Y9, Cb9, Cr9	Y5	Y9	G5
P12	Y4, Cb4, Cr4	Y8, Cb8, Cr8	Y4	Y8	G4
P11	Y3, Cb3, Cr3	Y7, Cb7, Cr7	Y3	Y7	G3
P10	Y2, Cb2, Cr2	Y6, Cb6, Cr6	Y2	Y6	G2
P9	Y1, Cb1, Cr1	Y5, Cb5, Cr5	Y1	Y5	G1
P8	Y0, Cb0, Cr0	Y4, Cb4, Cr4	Y0	Y4	G0
P7	High-Z	High-Z	Cb7, Cr7	Cb11, Cr11	B7
P6	High-Z	High-Z	Cb6, Cr6	Cb10, Cr10	B6
P5	High-Z	High-Z	Cb5, Cr5	Cb9, Cr9	B5
P4	High-Z	High-Z	Cb4, Cr4	Cb8, Cr8	B4
P3	High-Z	High-Z	Cb3, Cr3	Cb7, Cr7	B3
P2	High-Z	High-Z	Cb2, Cr2	Cb6, Cr6	B2
P1	High-Z	High-Z	Cb1, Cr1	Cb5, Cr5	B1
P0	High-Z	High-Z	Cb0, Cr0	Cb4, Cr4	B0

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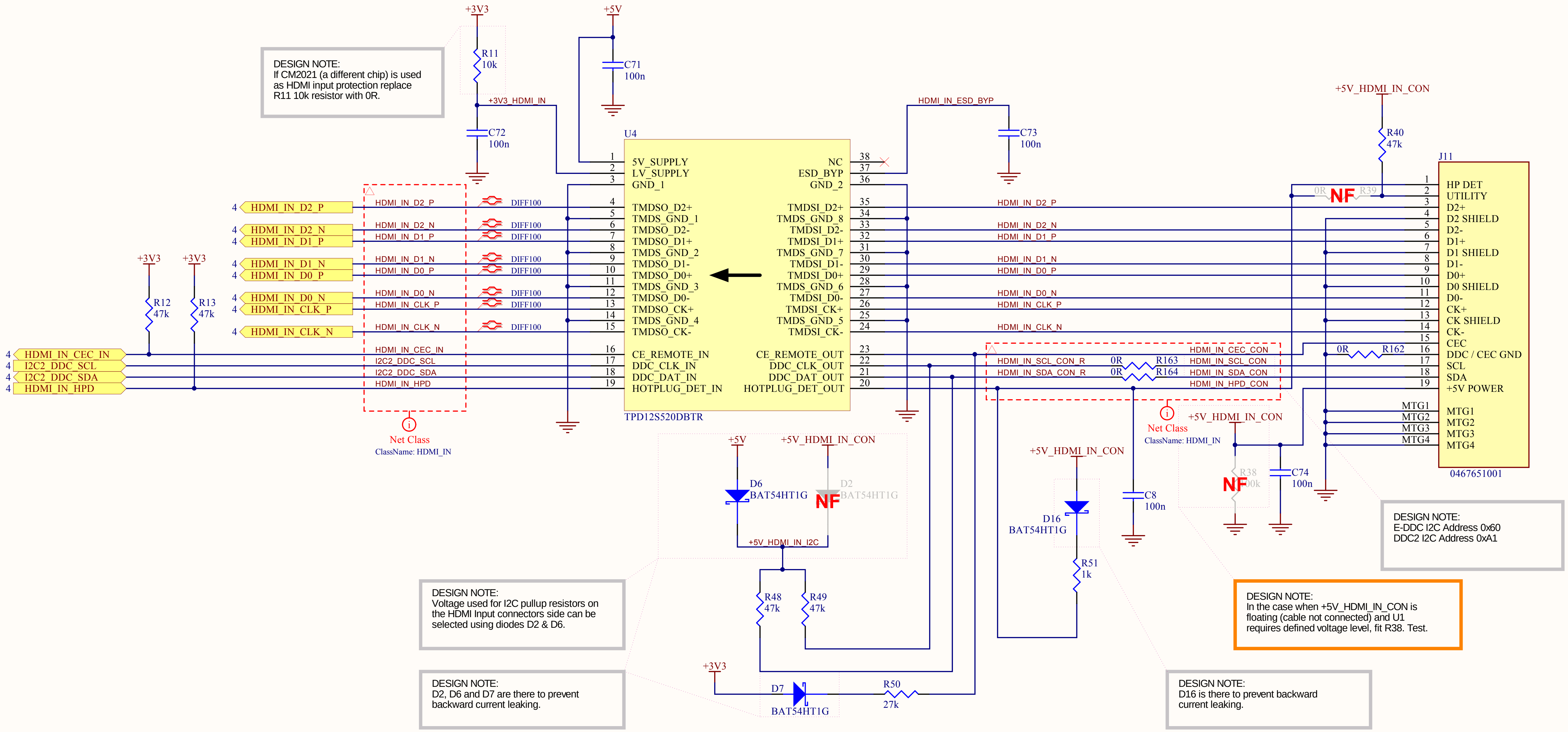
HDMI Input Connector



DESIGN NOTE:
If CM2021 (a different chip) is used as HDMI input protection replace R11 10k resistor with 0R.
+3V3
R11 10k
+3V3_HDMI_IN
C72 100n
+5V
C71 100n
U4
1 5V_SUPPLY
2 LV_SUPPLY
3 GND_1
4 TMDSO_D2+
5 TMDS_GND_1
6 TMDSO_D2-
7 TMDSO_D1+
8 TMDS_GND_2
9 TMDSO_D1-
10 TMDSO_D0+
11 TMDS_GND_3
12 TMDSO_D0-
13 TMDSO_CK+
14 TMDS_GND_4
15 TMDSO_CK-
16 CE_REMOTE_IN
17 DDC_CLK_IN
18 DDC_DAT_IN
19 HOTPLUG_DET_IN
38 NC
37 ESD_BYP
36 GND_2
35 TMDSI_D2+
34 TMDS_GND_8
33 TMDSI_D2-
32 TMDSI_D1+
31 TMDS_GND_7
30 TMDSI_D1-
29 TMDSI_D0+
28 TMDS_GND_6
27 TMDSI_D0-
26 TMDSI_CK+
25 TMDS_GND_5
24 TMDSI_CK-
23 CE_REMOTE_OUT
22 DDC_CLK_OUT
21 DDC_DAT_OUT
20 HOTPLUG_DET_OUT
TPD12S520DBTR
HDMI_IN_ESD_BYP
C73 100n
4 HDMI_IN_D2_P
4 HDMI_IN_D2_N
4 HDMI_IN_D1_P
4 HDMI_IN_D1_N
4 HDMI_IN_D0_P
4 HDMI_IN_D0_N
4 HDMI_IN_CLK_P
4 HDMI_IN_CLK_N
4 HDMI_IN_CEC_IN
4 I2C2_DDC_SCL
4 I2C2_DDC_SDA
4 HDMI_IN_HPD
R12 47k
R13 47k
DIFF100
Net Class
ClassName: HDMI_IN
+5V_HDMI_IN_CON
R40 47k
0R R39 NF
J11
1 HP DET
2 UTILITY
3 D2+
4 D2 SHIELD
5 D2-
6 D1+
7 D1 SHIELD
8 D1-
9 D0+
10 D0 SHIELD
11 D0-
12 CK+
13 CK SHIELD
14 CK-
15 CEC
16 DDC / CEC GND
17 SCL
18 SDA
19 +5V POWER
MTG1
MTG2
MTG3
MTG4
0467651001
0R R162
HDMI_IN_SCL_CON_R
HDMI_IN_SDA_CON_R
0R R163
0R R164
HDMI_IN_CEC_CON
HDMI_IN_SCL_CON
HDMI_IN_SDA_CON
HDMI_IN_HPD_CON
C8 100n
R38 100k NF
C74 100n
D6 BAT54HT1G
D2 BAT54HT1G NF
+5V_HDMI_IN_I2C
R48 47k
R49 47k
D7 BAT54HT1G
R50 27k
D16 BAT54HT1G
R51 1k
DESIGN NOTE:
Voltage used for I2C pullup resistors on the HDMI Input connectors side can be selected using diodes D2 & D6.
DESIGN NOTE:
D2, D6 and D7 are there to prevent backward current leaking.
DESIGN NOTE:
E-DDC I2C Address 0x60
DDC2 I2C Address 0xA1
DESIGN NOTE:
In the case when +5V_HDMI_IN_CON is floating (cable not connected) and U1 requires defined voltage level, fit R38. Test.
DESIGN NOTE:
D16 is there to prevent backward current leaking.

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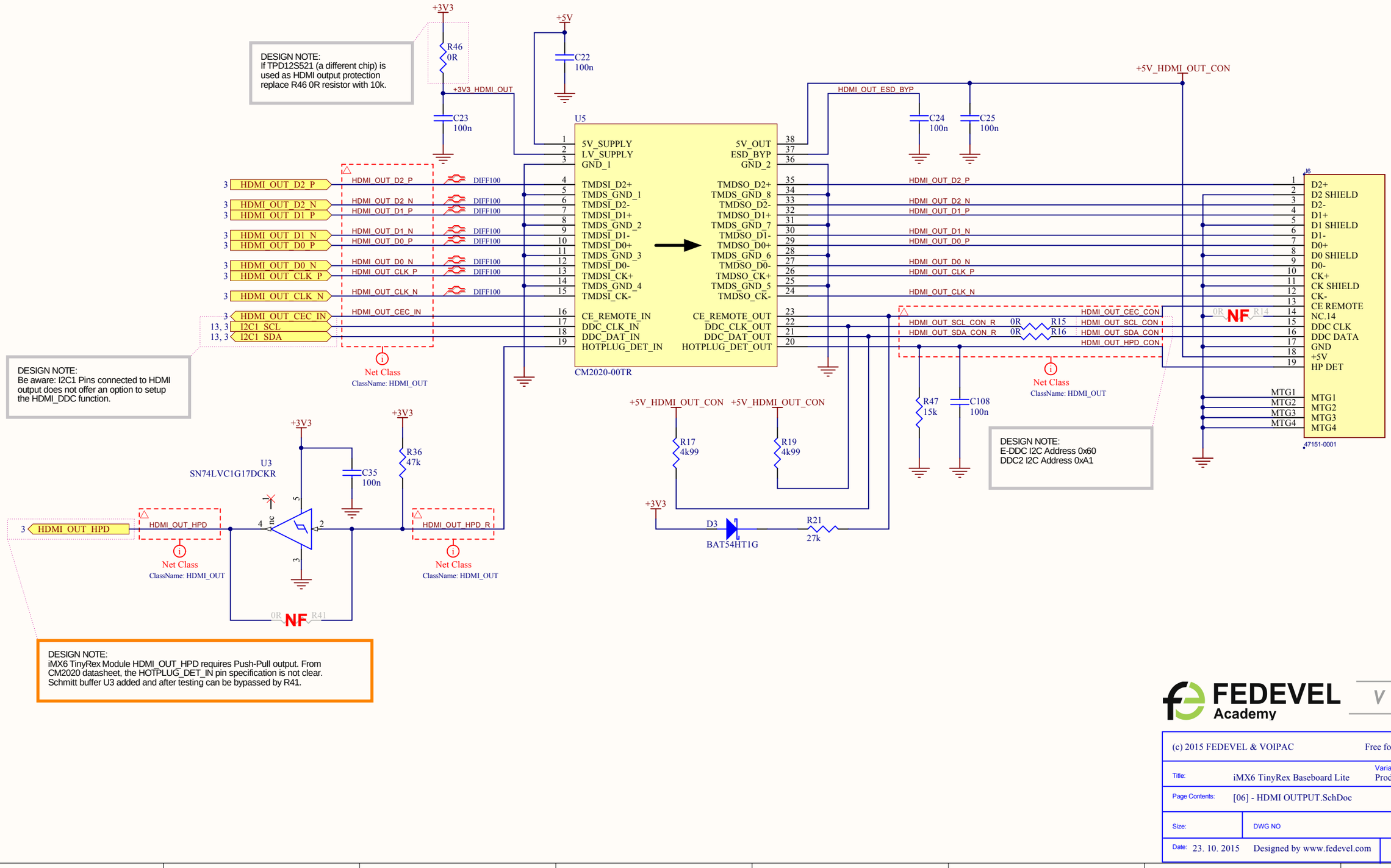
HDMI Output Connector



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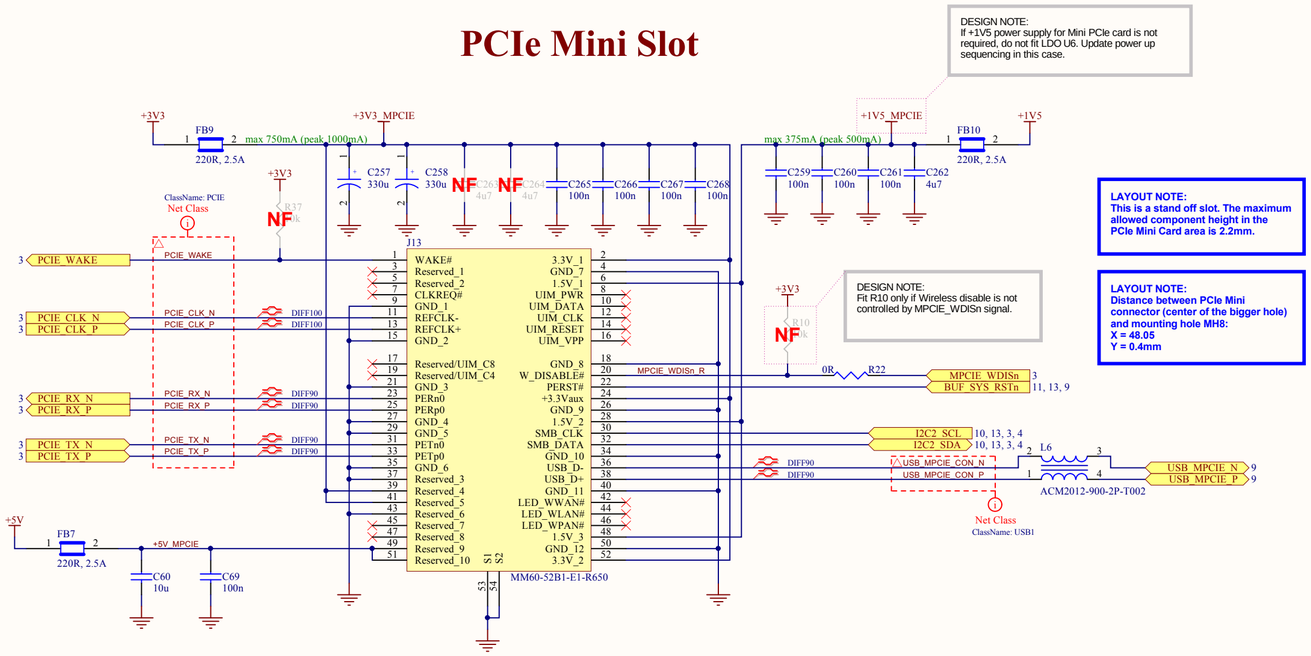
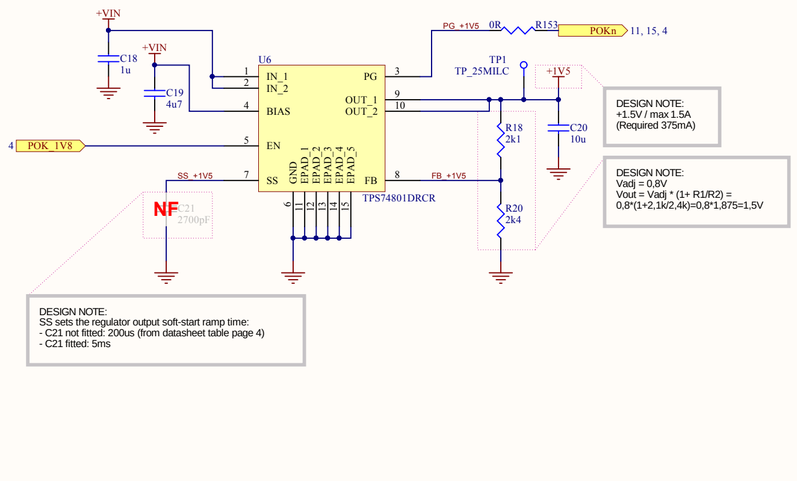
PCIE MINI

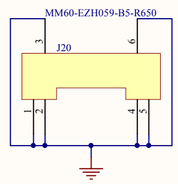
PCIe Mini Slot



PCIe Mini +1V5 power



PCIe Mini Card Latch



LAYOUT NOTE:
Distance between PCIe Mini connector and latch (hole to hole - the bigger ones):
X = 50.3mm
Y = 0.4mm

See also:
https://jae-connectors.com/en/pdf_download_exec.cfm?param=SJ105219.pdf

3D Model of PCIe Mini Card

CR1

Mini PCIe Card

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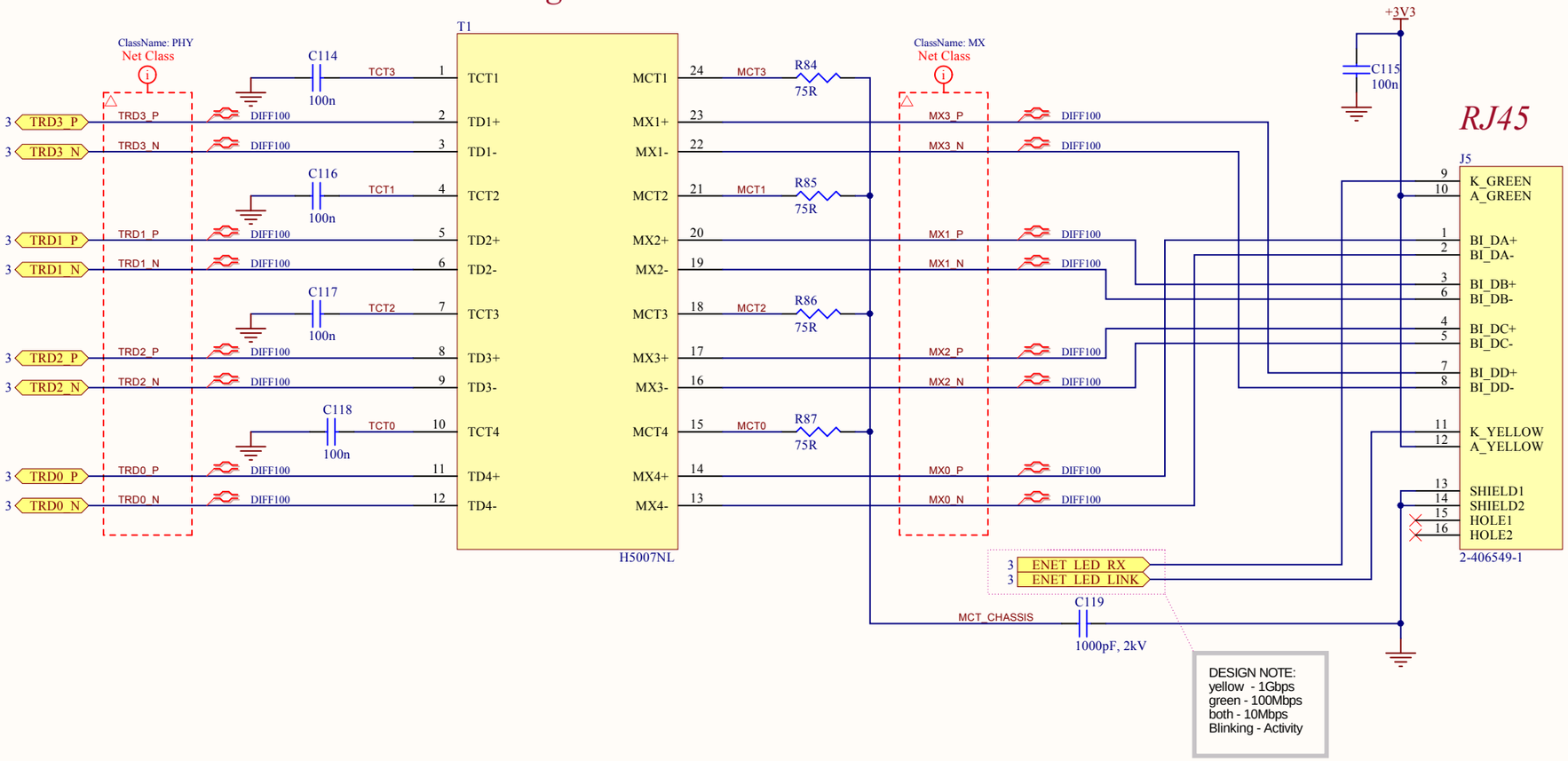
ETHERNET

Magnetics



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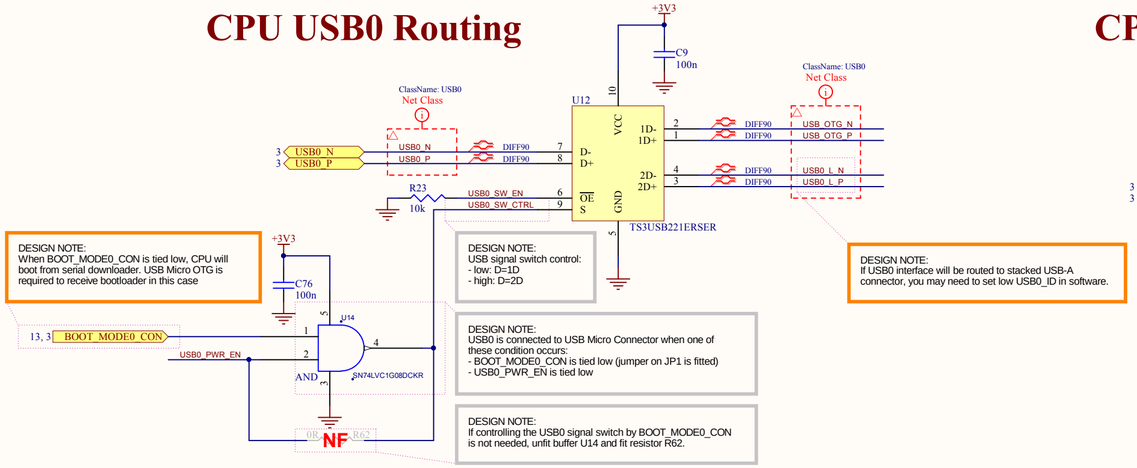
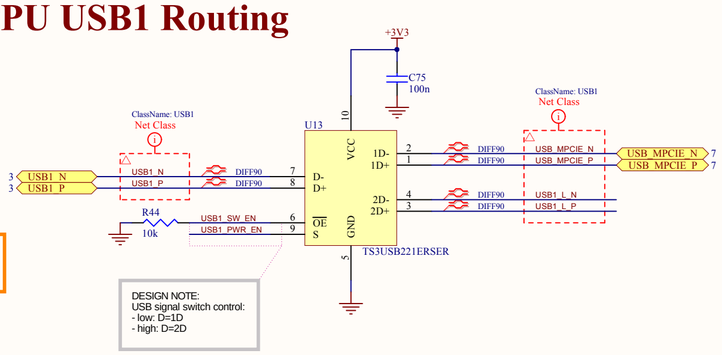
USB

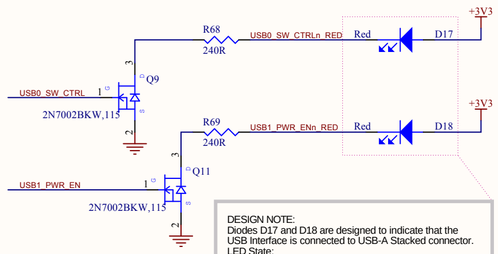
CPU USB0 Routing



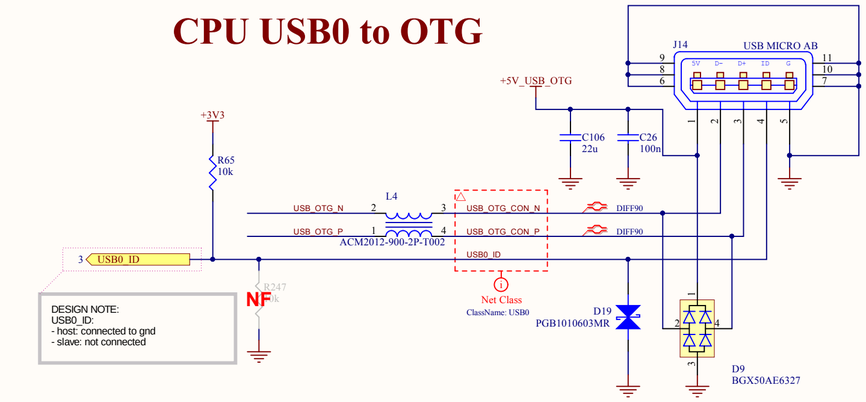
CPU USB1 Routing



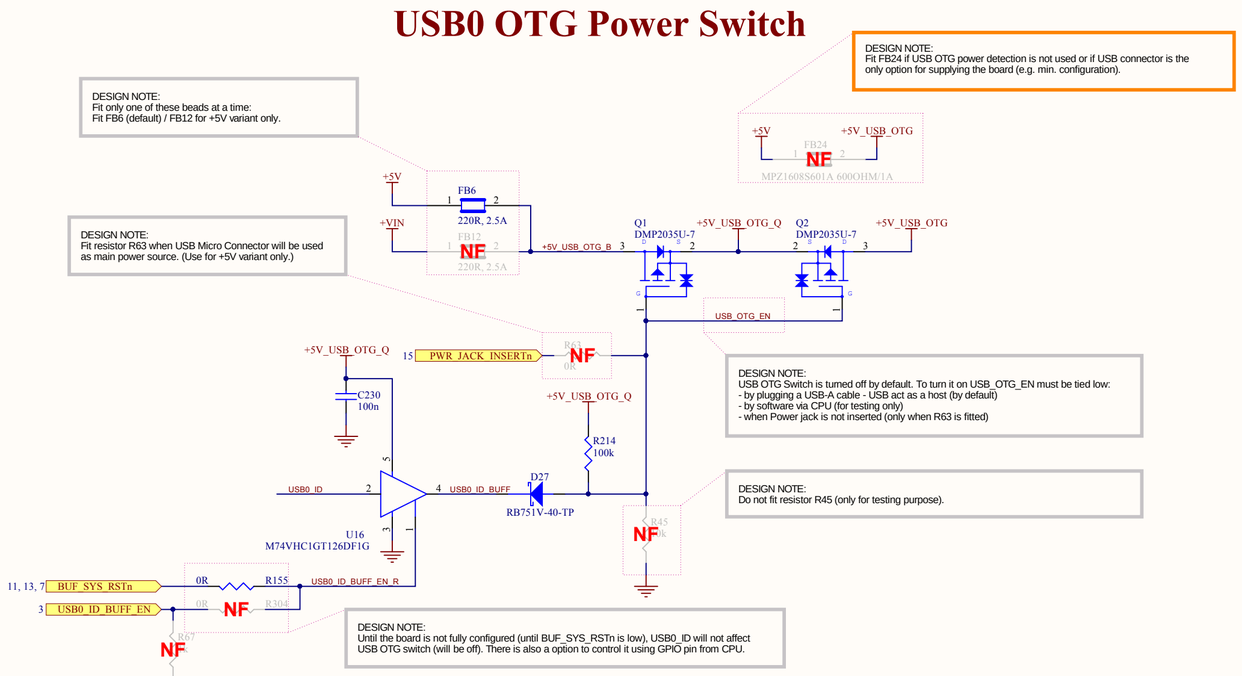
USB Switch LEDs



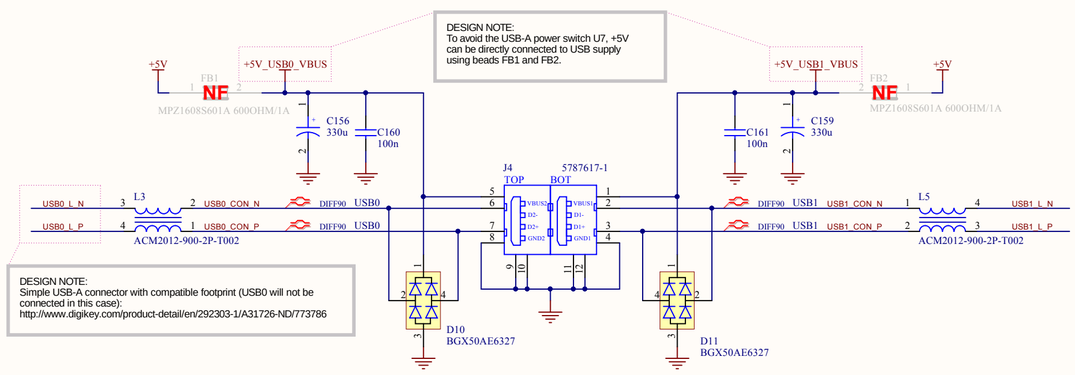
CPU USB0 to OTG



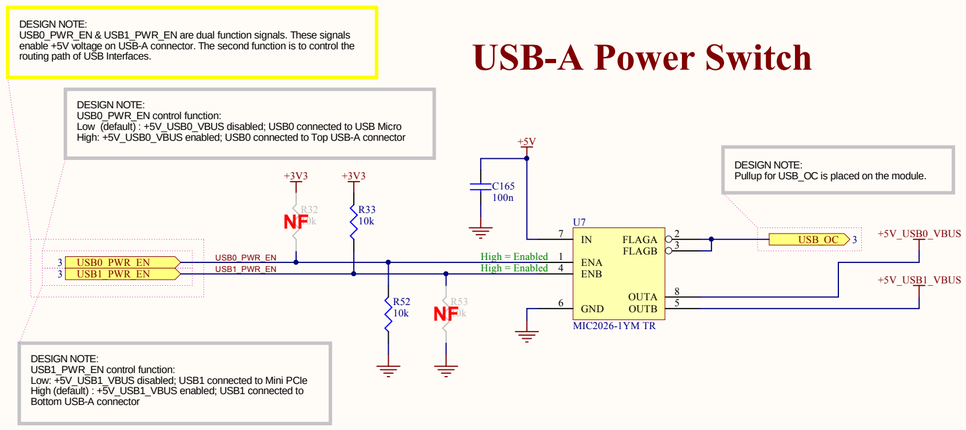
USB0 OTG Power Switch



USB-A Connector



USB-A Power Switch



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Title:	iMX6 TinyRex Baseboard Lite	Variant:	Production
Page Contents:	[09] - USB.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
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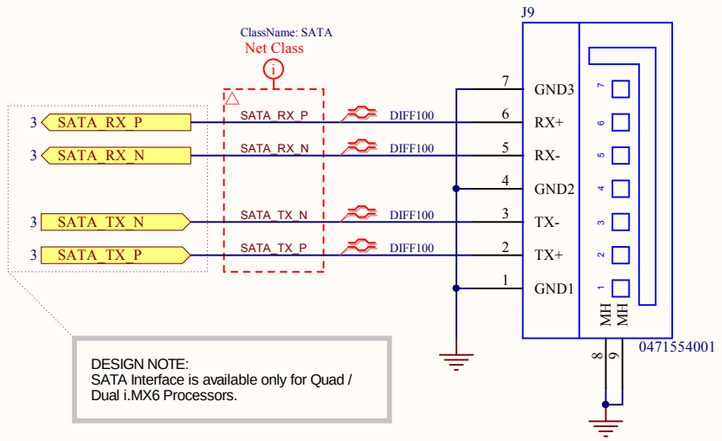
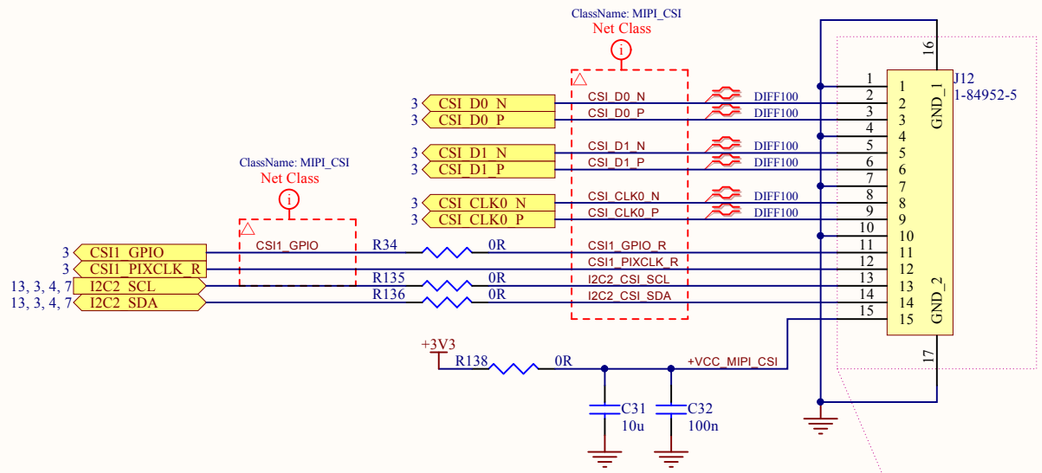
SATA, CSI

SATA



DESIGN NOTE:
SATA Interface is available only for Quad / Dual i.MX6 Processors.

MIPI CSI



DESIGN NOTE:
MIPI CSI connector is pin compatable with Raspberry Pi camera connector.

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Title:	iMX6 TinyRex Baseboard Lite	Variant: Production	
Page Contents:	[10] - SATA, CSI.SchDoc		Checked by
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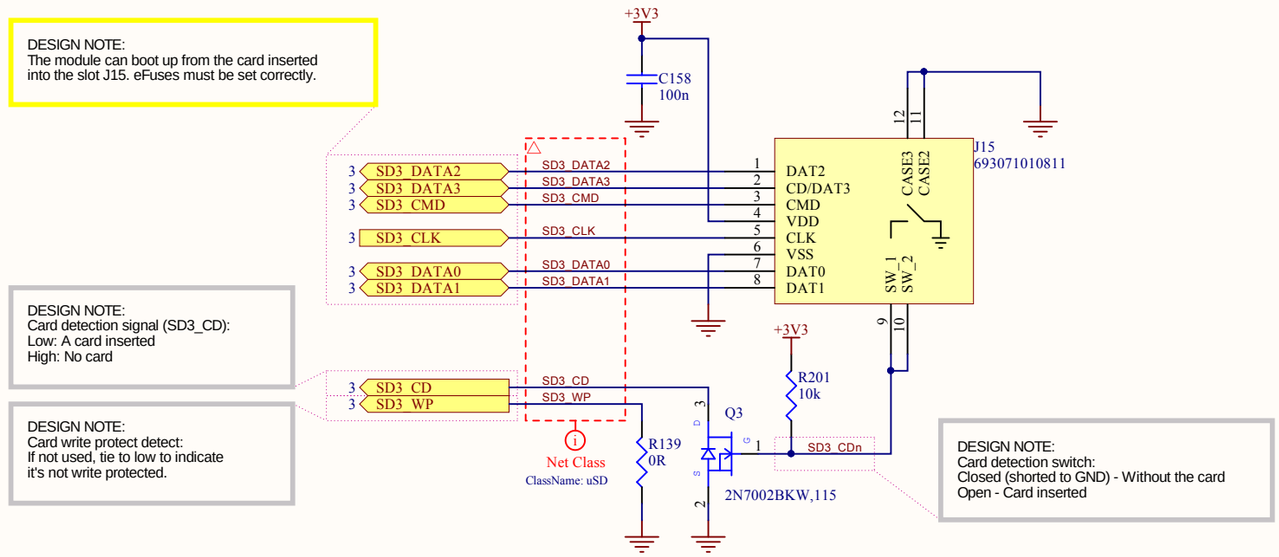
SD CARD, BUFFERS

Micro SD Slot

DESIGN NOTE:
The module can boot up from the card inserted into the slot J15. eFuses must be set correctly.

DESIGN NOTE:
Card detection signal (SD3_CD):
Low: A card inserted
High: No card

DESIGN NOTE:
Card write protect detect:
If not used, tie to low to indicate it's not write protected.



DESIGN NOTE:
Card detection switch:
Closed (shorted to GND) - Without the card
Open - Card inserted

3D Model of Micro SD Card

CR2

Micro SD Card

Micro SD Card

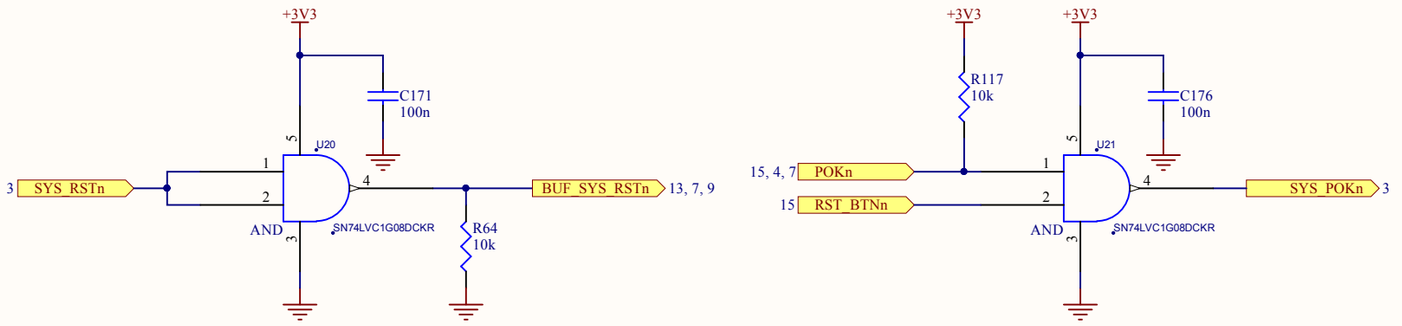
Software

FIRMWARE_FOR_CARD_IN_J15

FIRMWARE uBOOT + OS

iMX6 TinyRex uBOOT+OS 1.0

RESET BUFFERS



Title:	iMX6 TinyRex Baseboard Lite	Variant: Production
Page Contents:	[11] - SD CARD, BUFFERS.SchDoc	Checked by
Size:	DWG NO	Revision: V1I1
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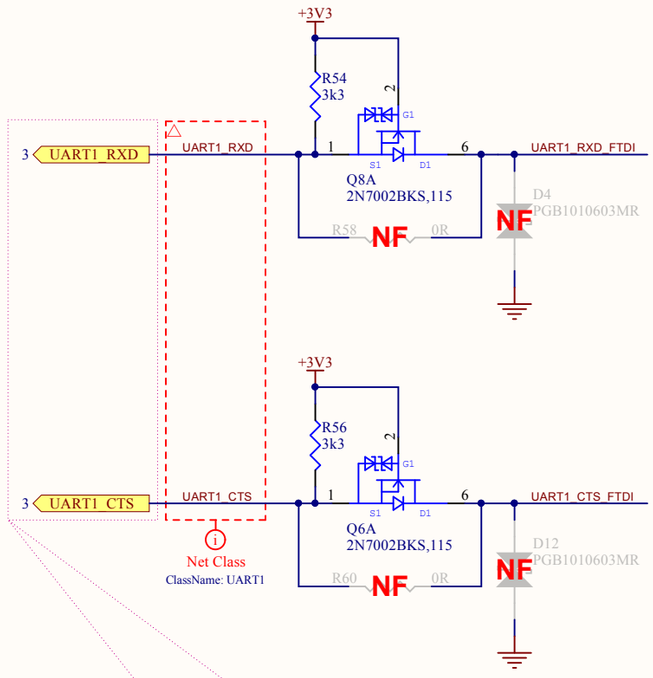
UARTS

UART 1 - Debug console (+3V3)

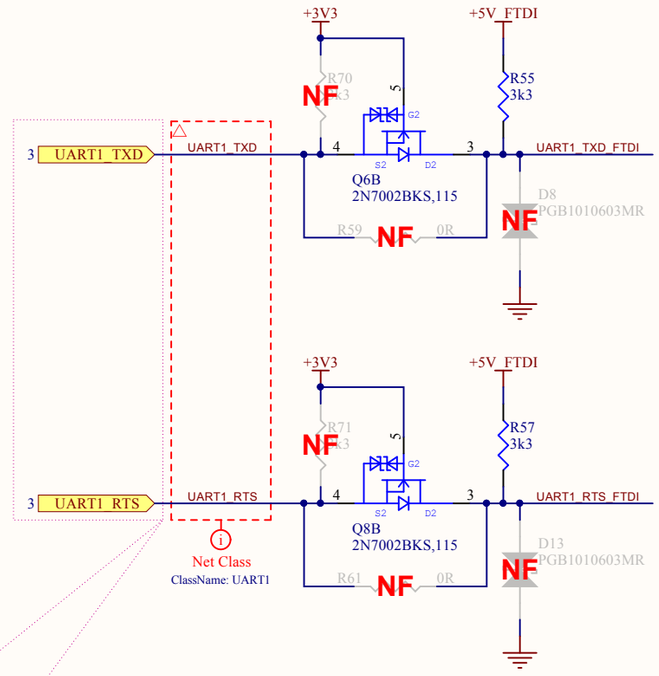
Buffers for CPU Input Pins



DESIGN NOTE:
Buffers for UART1 are designed to isolate the CPU when the board is turned off and cable is still connected. Without an isolation plugged cable can prevent CPU from booting.

DESIGN NOTE:
If isolation function is not needed, buffers can by bypassed using resistors R58-R61.

Buffers for CPU Output Pins

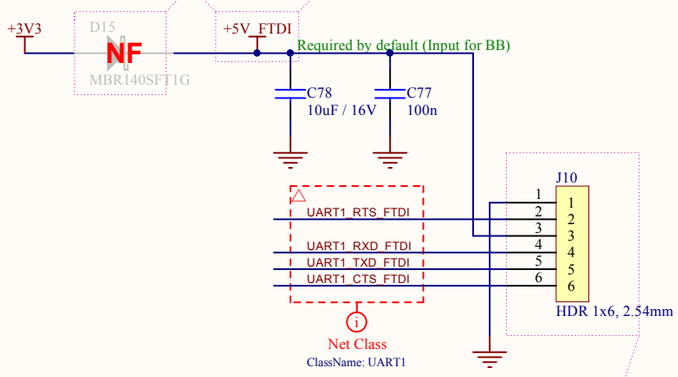


DESIGN NOTE:
If custom board / connector will be connector to J10, power voltage on J10-pin3 can be provided if UART level translation is desired.

When voltage translation is not needed, fit diode D15 insted. If diode is fitted, do not connect any power voltage to pin J10-3 although it can be used as a power output for add-on board (max 1A).

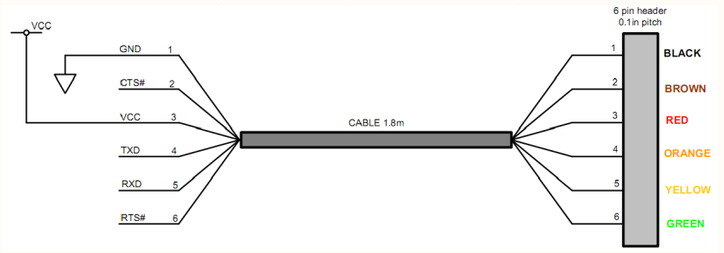
Serial console header

DESIGN NOTE:
To pin J10-3 can be also connected to a voltage with different level. UART signals from CPU to the cable will be translated to this voltage level.

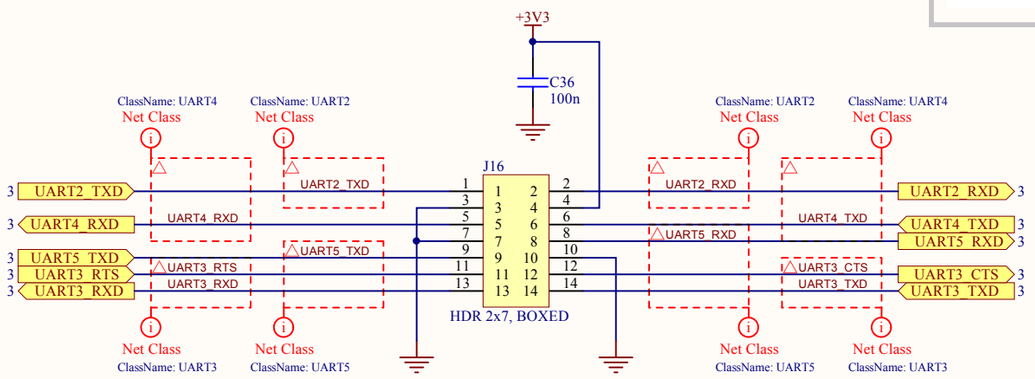


DESIGN NOTE:
Serial console header is designed to be used with FTDI TTL-232R-3V3 TTL to USB Serial Converter Cable by default:
http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_TTL-232R_CABLES.pdf

DESIGN NOTE:
FTDI TTL-232R-3V3 Cable Pinout (Left side - Converter; Right Side - iMX6 TinyRex)



UART Header



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Title:	iMX6 TinyRex Baseboard Lite	Variant:	Production
Page Contents:	[12] - UARTS.SchDoc		Checked by
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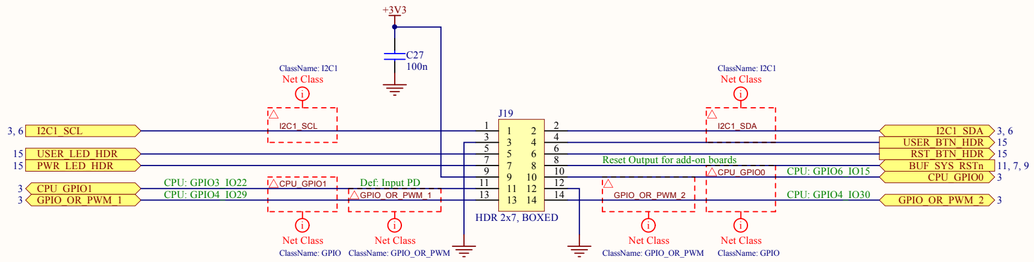
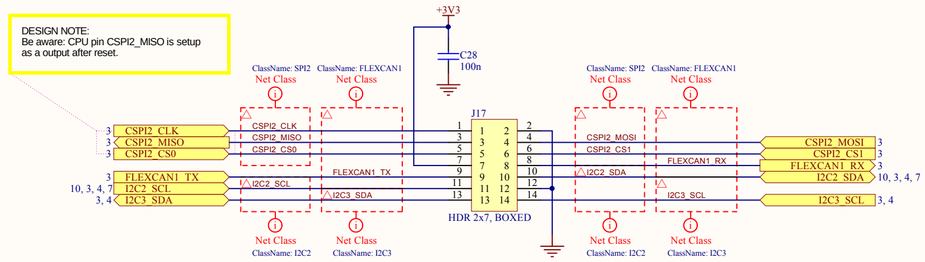
HEADERS, SPI

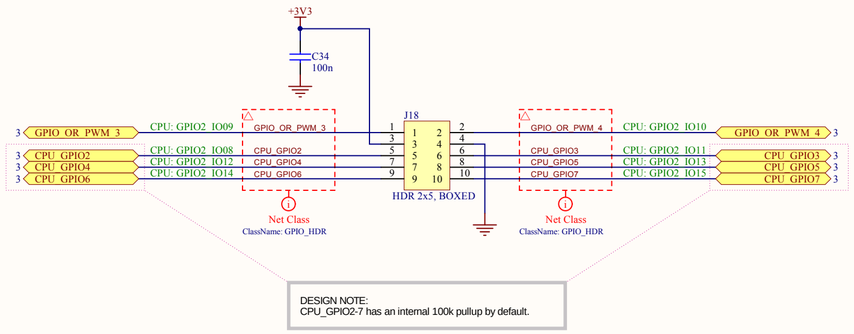
SYSTEM HEADER



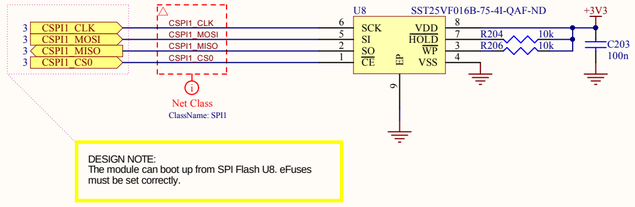
PERIPHERAL HEADER



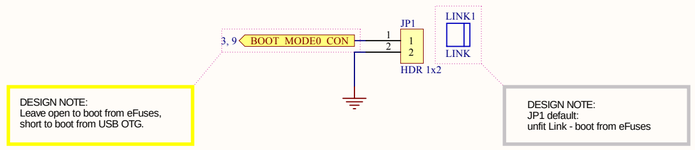
GPIO & PWM HEADER



SPI NOR FLASH



BOOT MODE SELECTION



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Title:	iMX6 TinyRex Baseboard Lite	Variant: Production
Page Contents:	[13] - HEADERS, SPI.SchDoc	Checked by
Size:	DWG NO	Revision: V1I1
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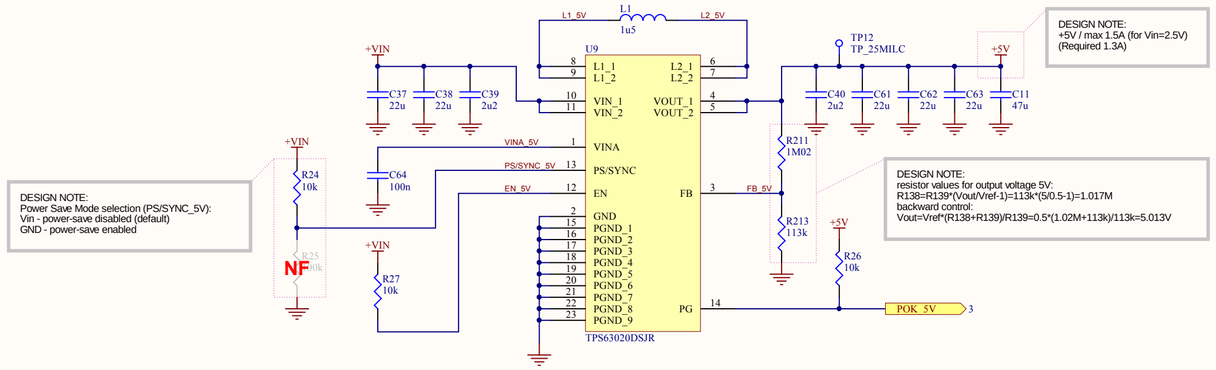
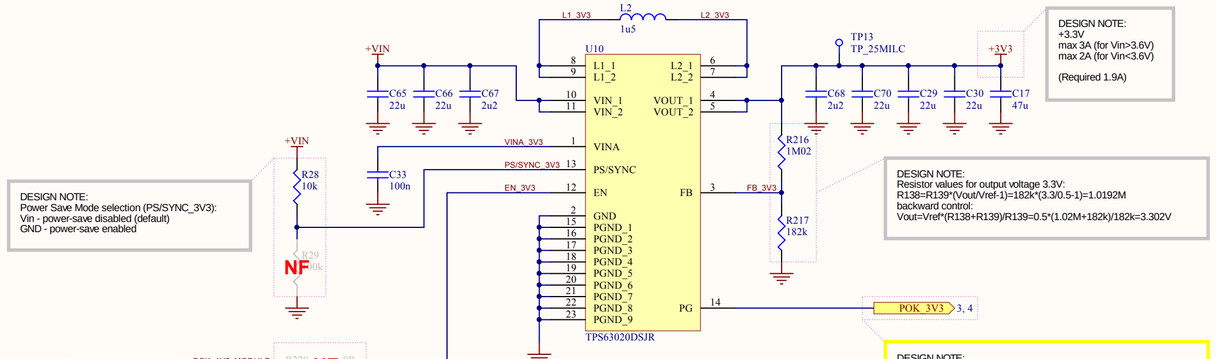
POWERS +5V, +3V3, +2V5

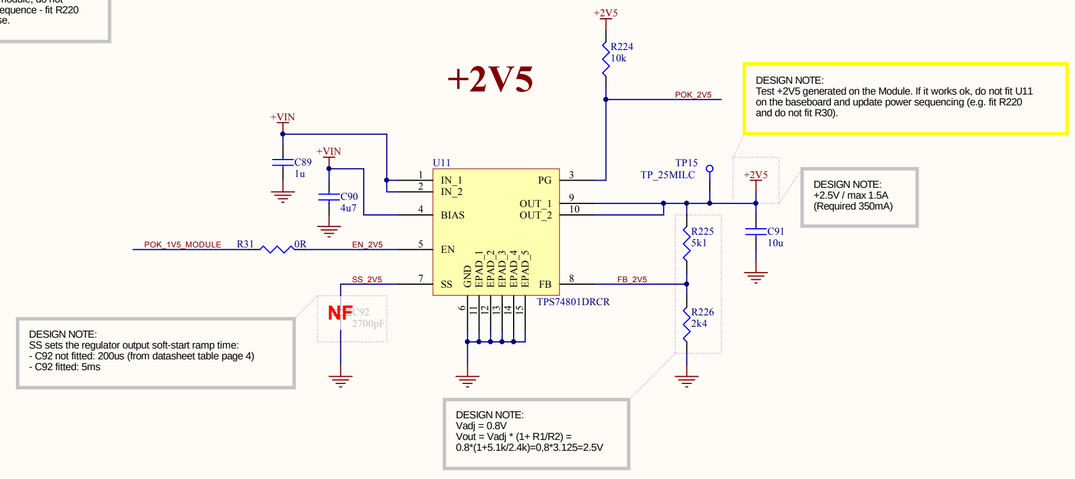
+5V



+3V3



+2V5



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Title:	iMX6 TinyRex Baseboard Lite	Variant:	Production
Page Contents:	[14] - PWR 5V, 3V3, 2V5.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
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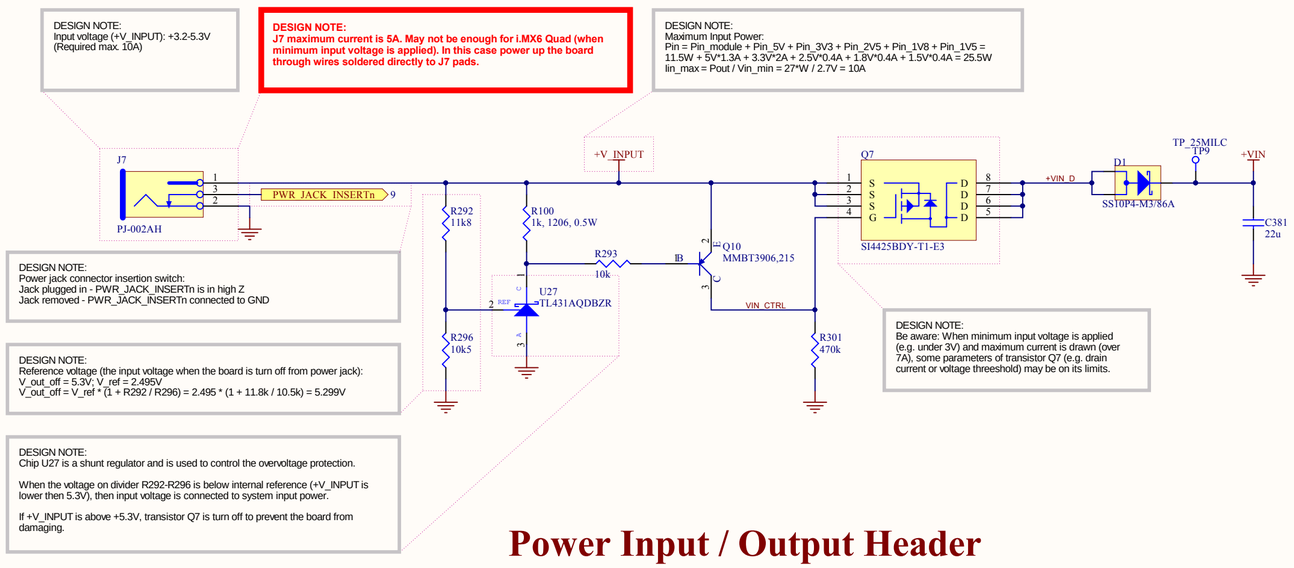
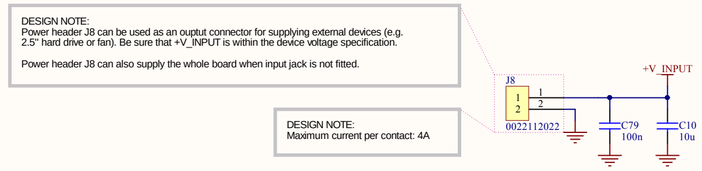
PWR IN, LEDS, BUTTONS, MECH

Power Input (+3.2 to +5.3V DC)

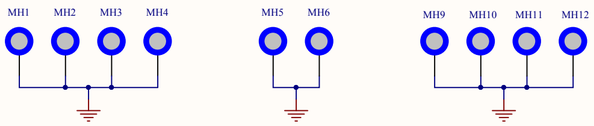


Power Input / Output Header



Mechanical

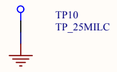
Mounting Holes



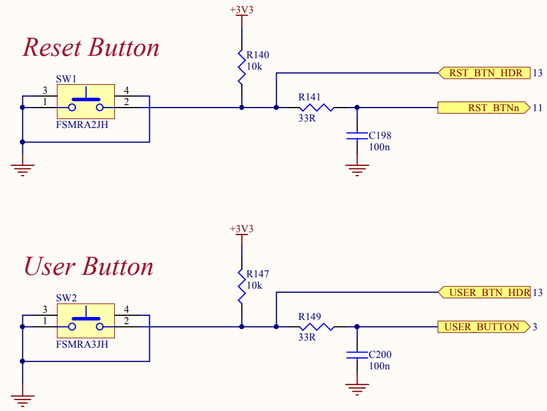
Module Mounting Accessories

Fiducials

Gnd Testpoint

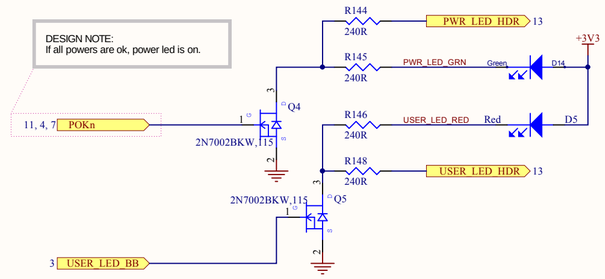


Buttons



LEDs

Power & User LEDs



PCB

PCB1

PCB

iMX6 TinyRex Baseboard Lite V1I1 PCB

iMX6 TinyRex Module 3D Model

M1

3D Model

iMX6 TinyRex Module V1I1 3D

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Title: iMX6 TinyRex Baseboard Lite	Variant: Production	
Page Contents: [15] - PWR IN, LEDS, BUTTONS, MECH.SchDoc	Checked by	
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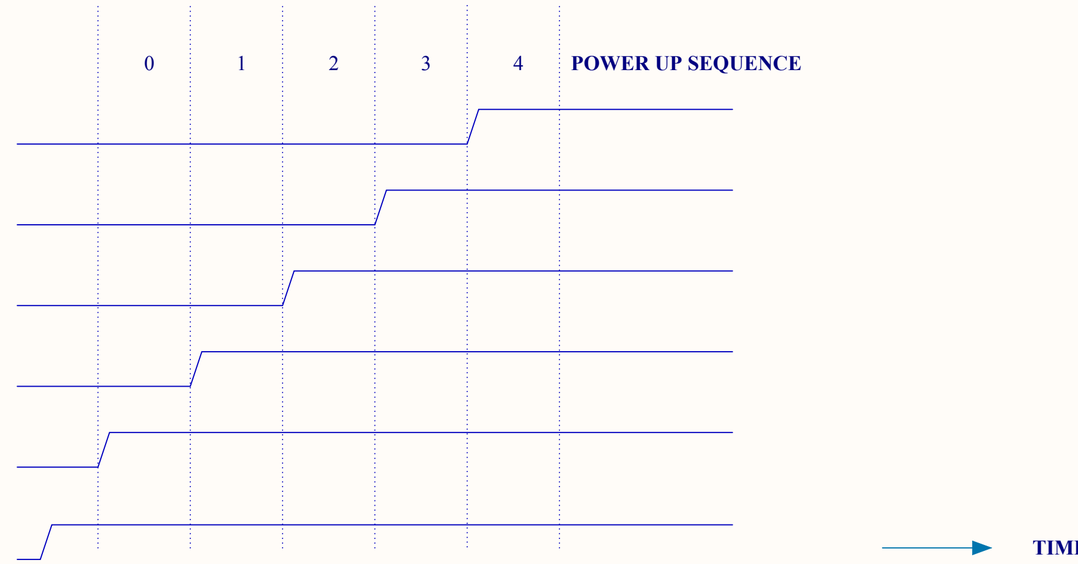
DOC, POWER SEQUENCING

Power Sequencing

CONTROLED BY	NAME	LEVEL	USED BY
POK_1V8	+1V5	1.5V	PCIe Mini Card
POK_3V3	+1V8	1.8V	Video input chip
POK_2V5	+3V3 *1	3.3V	Module, Peripherals
POK_5V (J2-pin 7) -> POK_3V0 -> -> POK_1V375 -> POK_1V5 (J2-pin 5) *2	+2V5 *3	2.5V	Module
	+5V *1	5V	Module, USB, PCIE Mini Card
	+VIN *1	3.2V-5.3V	Module, Power supplies



DESIGN NOTE:
***1 These power rails must be provided for the module**
***2 This signal is provided by the module**

*3 This power rail can be generated on the module. Testing required

I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
I2C1	*HDMI Output*	*0x60 , 0xA1*
	EEPROM (on module)	*0xAE/0xAF*
	For general use (on header J19)	
I2C2	*HDMI Input*	*0x60 , 0xA1*
	HDMI Input Chip	*0xA0 , 0x74*
	Mini PCIe Card	
	MIPI CSI connector	
	For general use (on header J17)	
I2C3	*HDMI Input Chip Control*	*0x98/0x9A*
	For general use (on header J17)	

License

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Title:	iMX6 TinyRex Baseboard Lite	Variant: Production	
Page Contents:	[16] - DOC, POWER SEQUENCING.SchDoc		Checked by
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REVISION HISTORY

Title:	iMX6 TinyRex Baseboard Lite	Variant: Production	
Page Contents:	[17] - REVISION HISTORY.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
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Designator
[01] - COVER PAGE.SchDoc

Designator
[02] - BLOCK DIAGRAM.SchDoc

Designator
[03] - CONNECTORS.SchDoc

Designator
[04] - VIDEO INPUT.SchDoc

Designator
[05] - HDMI INPUT.SchDoc

Designator
[06] - HDMI OUTPUT.SchDoc

Designator
[07] - PCIE MINI.SchDoc

Designator
[08] - ETHERNET.SchDoc

Designator
[09] - USB.SchDoc

Designator
[10] - SATA, CSI.SchDoc

Designator
[11] - SD CARD, BUFFERS.SchDoc

Designator
[12] - UARTS.SchDoc

Designator
[13] - HEADERS, SPI.SchDoc

Designator
[14] - PWR 5V, 3V3, 2V5.SchDoc

Designator
[15] - PWR IN, LEDS, BUTTONS, MECH.SchDoc

Designator
[16] - DOC, POWER SEQUENCING.SchDoc

Designator
[17] - REVISION HISTORY.SchDoc

NOTES

Mark Not Fitted Components as
NF

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

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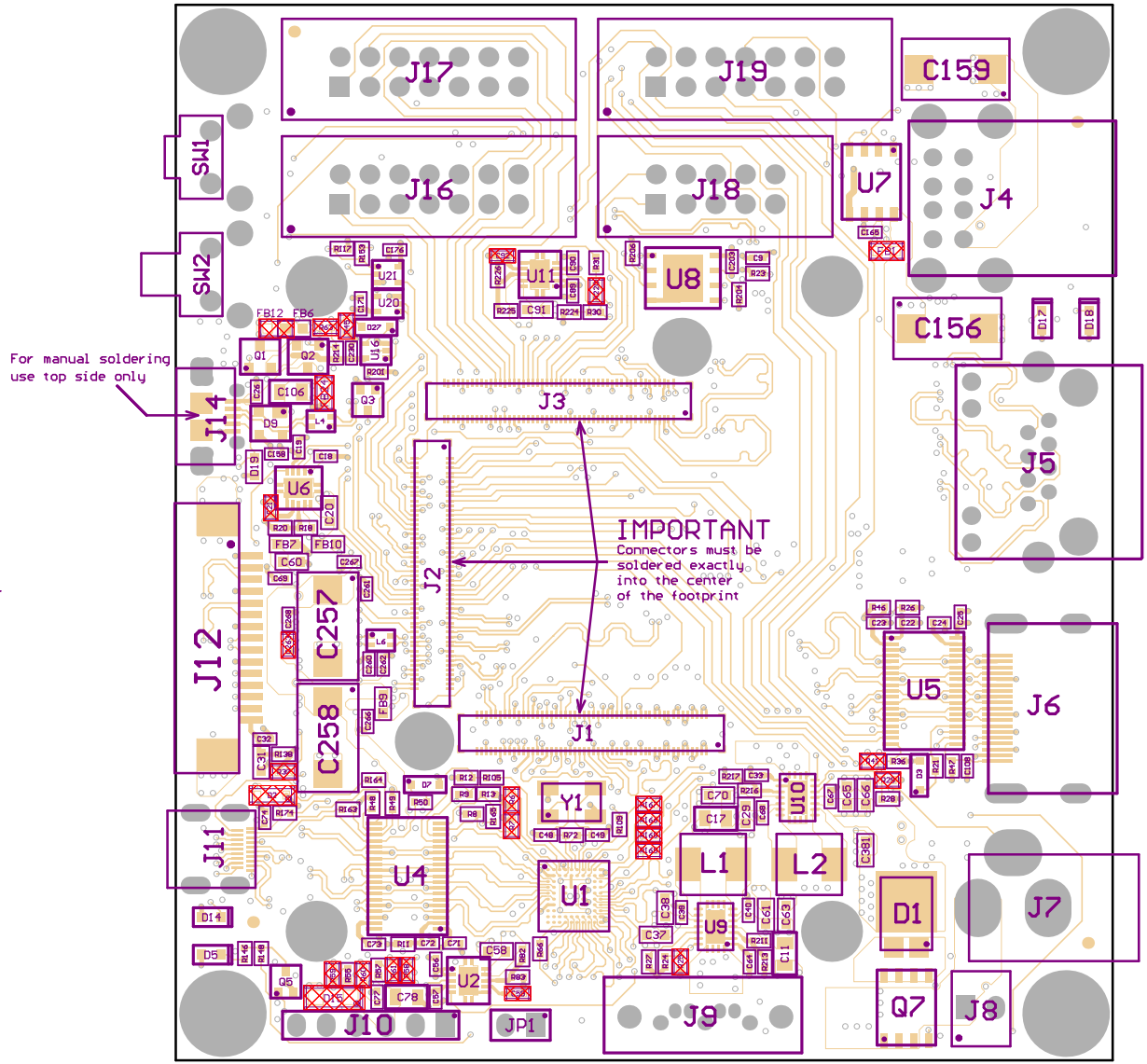
Title:	iMX6 TinyRex Baseboard Lite	Variant: Production	
Page Contents:	iMX6 TinyRex Baseboard Lite_V1I1 Project.SchDoc	Checked by	
Size:	DWG NO	Revision: V1I1	
Date: 23. 10. 2015	Designed by www.fedevel.com	Sheet 18 of 18	

Assembly TOP of iMX6 TinyRex Baseboard Lite V1I1

Production



Assembly BOTTOM of iMX6 TinyRex Baseboard Lite V1I1

Production