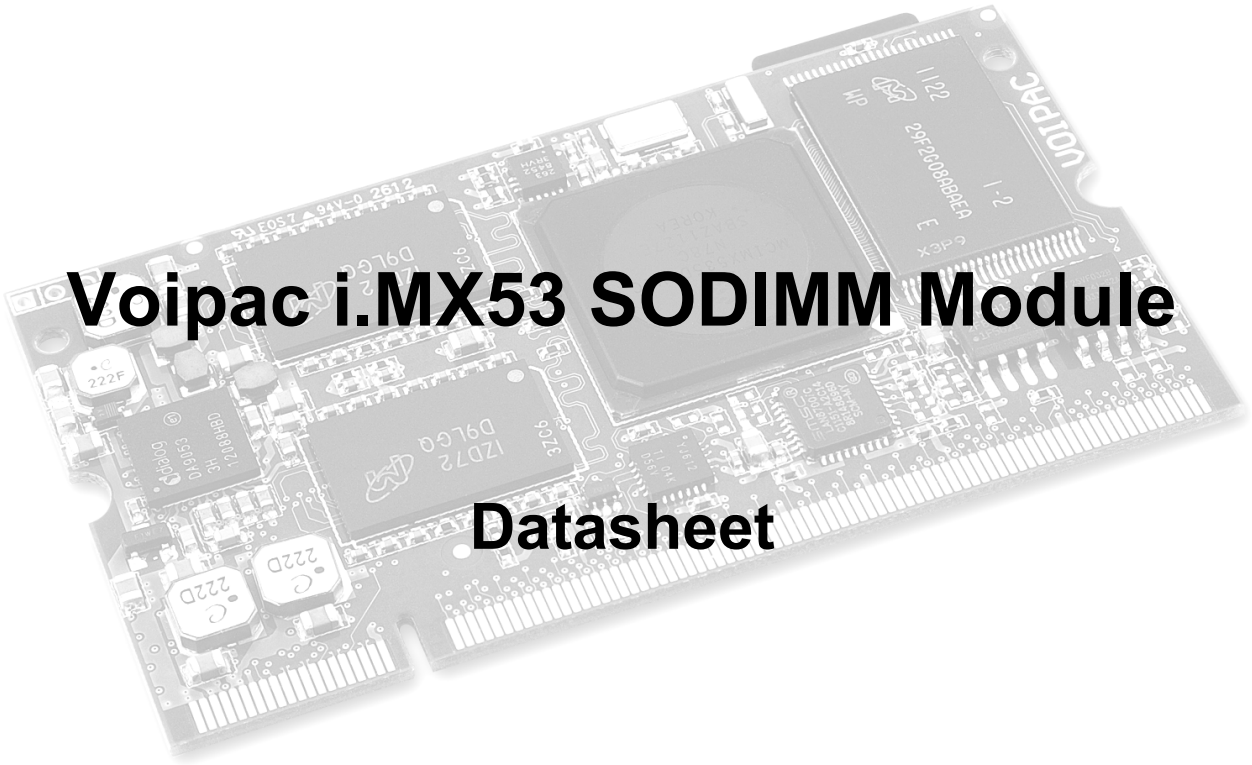


Voipac i.MX53 SODIMM Module

Datasheet

Date	Revision	Changes
20. April 2012	1.0	Initial Release
17. October 2012	1.1	Modified Power Consumption Table in Chapter 5.1 Modified Chapter 6.1

Table of Contents

1. Introduction

1.1. Hardware

The i.MX53 SODIMM Module represents the next generation of advanced multimedia, power-efficient and cost-effective solution for embedded systems. With preinstalled operating system and running up to 1.2GHz, the module enables designing of high-end products with quick set-up and easy-to-handle programming of own applications.

The highly integrated i.MX53 SODIMM Module is the third member of growing family of Voipac cross compatible COMs (Computers On Module) that are specially designed for use in the same peripheral-rich i.MX25 SODIMM Base Board, allowing the newly designed system to be tuned for price and performance, and re-use of the gathered knowledge as well as code.

The core component is the high-performance Freescale's i.MX53 advanced multimedia processor with very low power consumption. Only 1mm thick 10-layer HDI micro-via PCB board carries CPU, Flash, SDRAM, Ethernet and other chips thus providing vast majority of the embedded systems must-have peripherals. Usage of the Voipac's i.MX53 SODIMM Module saves many man-months of the high-frequency PCB design, complex prototyping, debugging and OS porting, thus minimizes the time-to-market of the customers' own applications.

The i.MX53 SODIMM format 200pin Module is available in 3 standard hardware configurations: BASIC / PROfesional / MAXimum. Upon request, any other possible configuration can be manufactured for no surcharge, minimum batch size is 10pcs. The operating temperature range of a standard unit is -20 to 70°C. Upon request, the module is available in -40 to 85°C operating temperature range for a surcharge, or in 0°C to +70°C commercial temperature range for a discounted price. For batches exceeding 100pcs, Voipac provides free service of the customer's own boot loader preloading prior to the order dispatch. The standard i.MX53 SODIMM Module is equipped by i.MX535 ARM Cortex A8™ CPU, thus supporting all of the available CPU features such as integrated display controller, full HD capability, enhanced graphics and connectivity.

As the only manufacturer in the embedded COM segment, Voipac provides free and complete schematic of its SODIMM sized Computers on Module to every complete development kit purchased.

The i.MX53 CPU officially launched in February 2011 belongs to the group of CPUs included in the Freescale Product Longevity Program, that guarantees a minimum availability of this CPU for a period of 15 years.

1.2. Software

Various operating systems are available for the Voipac i.MX53 SODIMM Module provided by Voipac and the third parties. In case of unsupported operating system, necessary documentation for all hardware peripherals is freely available.

Voipac fully supports Linux operating system with drivers for all basic interfaces. Custom additional drivers for specific applications can be developed upon request.

Operating system	Description
Linux	Linux 2.6 with drivers for most common interfaces
Android	Android Gingerbread 2.3 (OPTIONAL)
Windows CE	

1.3. Features Summary

Feature	Description
CPU	i.MX535 ARM Cortex-A8™ CPU (Freescale), clocked up to 1.2 GHz
DDR3 SDRAM	Up to 2GB
NAND FLASH	Up to 32GB
I2C EEPROM	Up to 512kB
SPI FLASH	Up to 8MB
LCD	LCD controller supporting UXGA 1600x1200px
AUDIO/TOUCH	Digital Audio IN/OUT, 4-wire touch controller
VIDEO CAPTURE	Still-Picture camera interface
VIDEO	HD Video encoder/decoder
MULTIMEDIA	• DDS – Dual Display Support • Dual Camera Interface • Hardware accelerated image processing • NEON SIMD media accelerator • GPU 3D – OpenGL ES 2.0 • GPU 2D – OpenVG 1.1
ETHERNET	LAN8700 10/100Mbps
USB	High-Speed USB 2.0 OTG/HOST
OTHER I/O	3xUART / 2xSDIO / I2C / SPI / EIM / GPIO / 2xSSI / AC97 / I2S

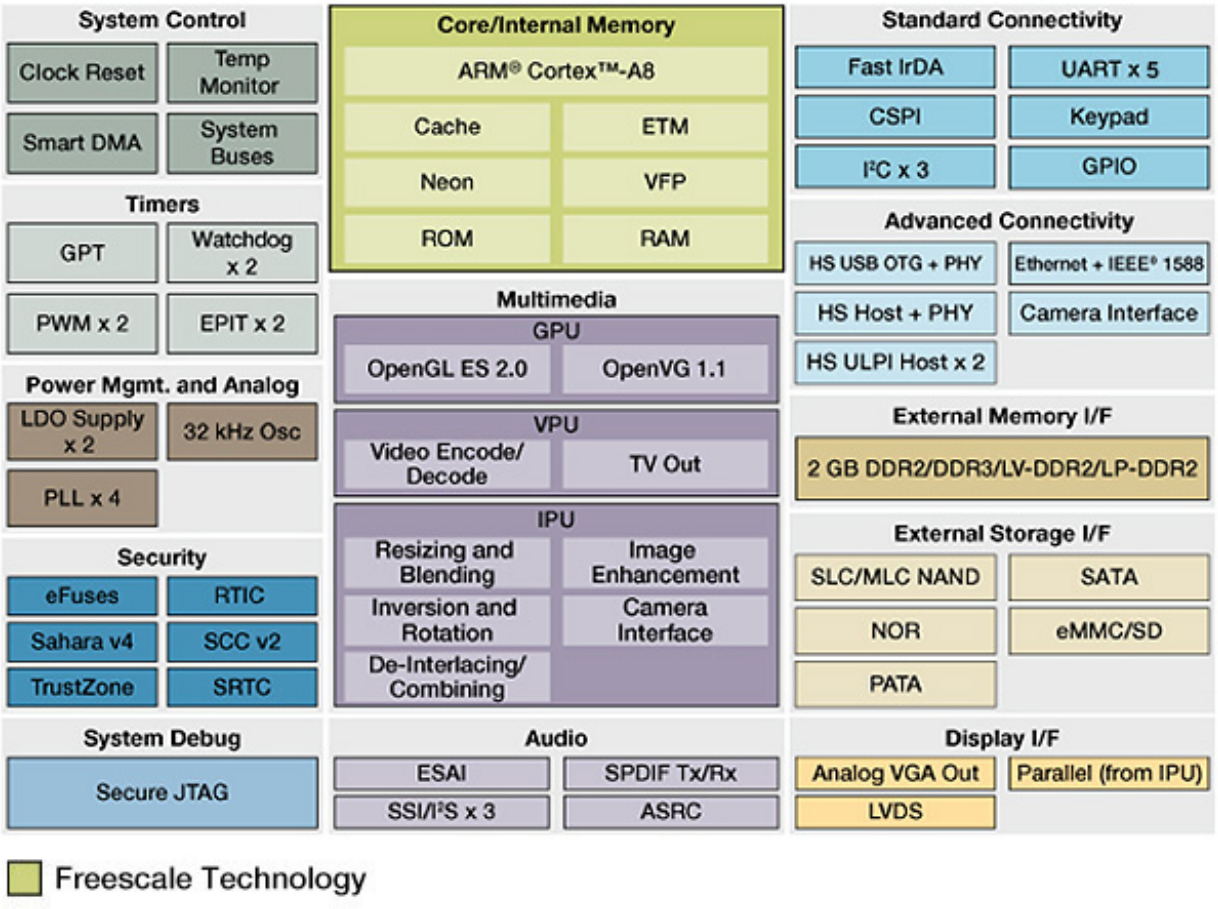
1.4. Reference Documents

For more detailed technical information about the i.MX53 SODIMM Module components, please refer to the web resources and documents listed below.

Component	Description
i.MX53 (Freescale) Processor	Freescale_data_sheet_iMX53.pdf
MICRON NAND Flash Memory	MT29F1G08ABADAWP-IT, MT29F2G08ABAEAWP-IT, MT29F4G08ABADAWP-IT
MICRON SDRAM Memory	MT41J128M16HA-15E, MT41J128M16HA-15E AAT, MT41J128M16HA-15E AIT, MT41J128M16HA-15E IT, MT41J256M16RE-15E, MT41J256M16RE-15E IT, MT41J64M16JT-15E, MT41J64M16JT-15E AAT, MT41J64M16JT-15E IT
SMSC LAN8700 Ethernet Controller	SMSC LAN8700.pdf
Power Management	DA9053-3HC51
I2C EEPROM	Atmel AT24C512BN-SH-B.pdf

2. Functional Processor Description

2.1. Block Diagram



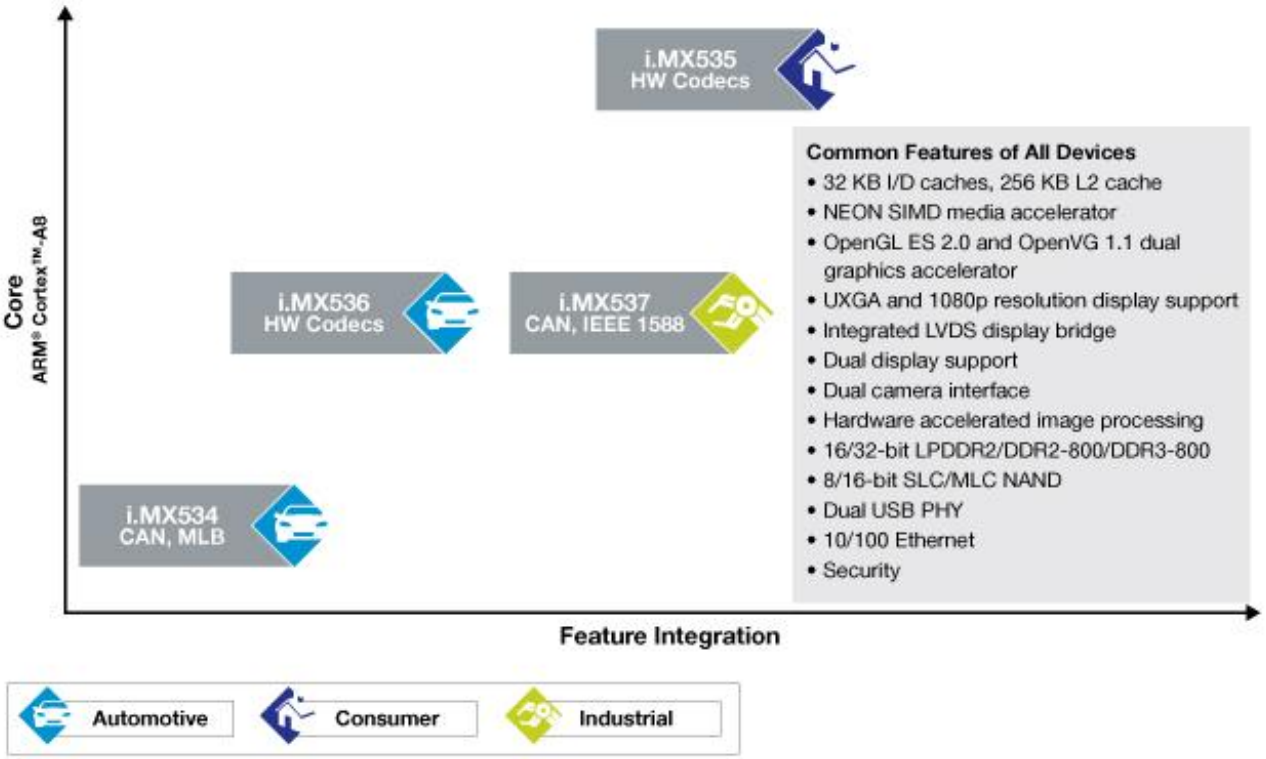
More information in interactive table on Freescale's webpage

The i.MX535 processor features Freescale's advanced and power-efficient implementation of the ARM Cortex A8™ core, which operates at speeds as high as 1,2 GHz. Up to 200 MHz DDR2 and mobile DDR DRAM clock rates are supported. The CPU is suitable for the following applications:

• **Tablets**	• **Smart Monitors**
• **Gaming Equipment**	• **Digital Signage**
• **Mobile Phones**	• **Telehealt System**
• **Voice Over Internet Protocol**	• **Advanced HMI**

More information in interactive table on Freescale's webpage

2.2. Features



i.MX534	
Up to 800 MHz	
Target Applications:	– Advanced HMI – Navigation – Instrument Cluster – Telematics

i.MX535	
Up to 1 GHz (Consumer)	
Target Applications:	– Tablet – Thin Client – Video IP Phone – Advanced HMI – Telehealth – Connected TV – Digital signage

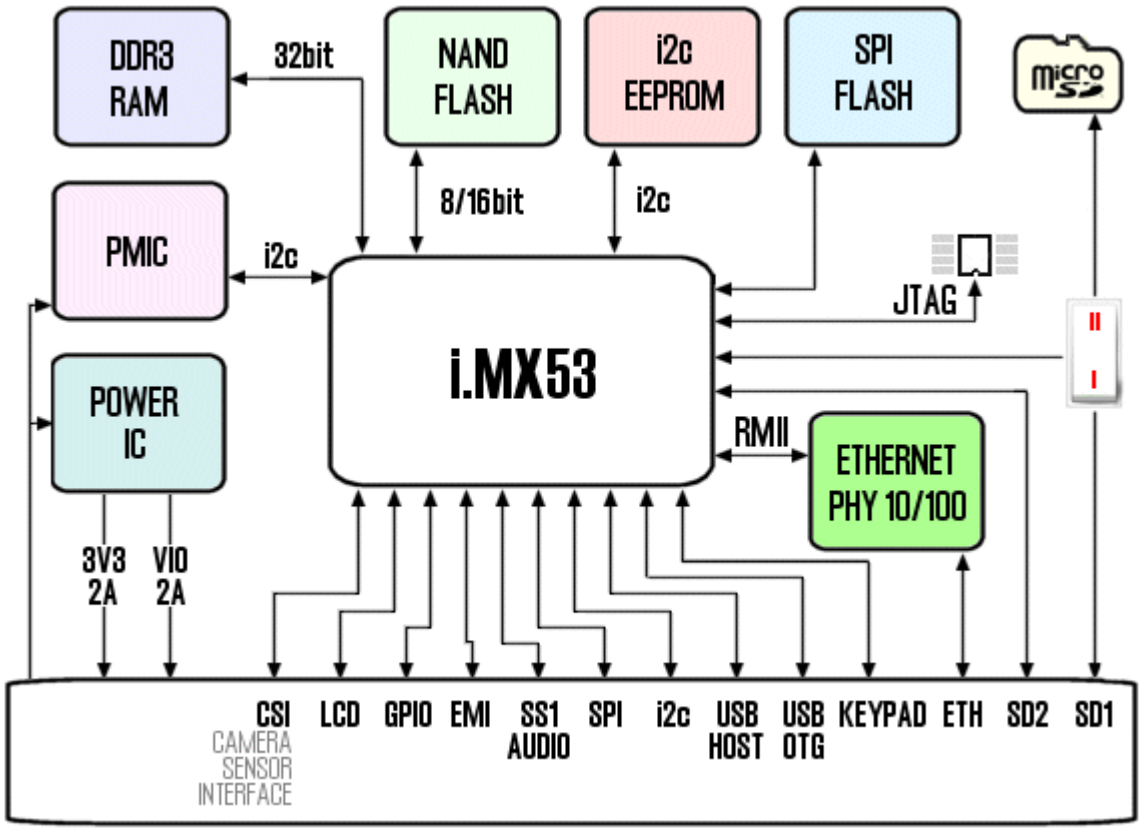
i.MX536	
Up to 800 MHz	
Target Applications:	– Infotainment – Rear Seat Entertainment

i.MX537	
Up to 800 MHz (Industrial)	
Target Applications:	– HMI for appliances, automation, printers, building controls – Patient Monitors – Point of Sales Terminals – Telematics – Telehealth – Digital signage

3. SODIMM Signal Description

This chapter describes the signals of the Voipac i.MX53 SODIMM Module. Some pins have dedicated functionality, but most are highly multiplexed, so that the same pin can have up to 6 different roles and the same functionality is sometimes available alternatively on different pins. Each of these multiplexed pins is additionally also usable as a General Purpose Input/Output pin (GPIO). Additionally each GPIO pin can be used as interrupt source.

3.1. SODIMM Module Block Diagram



3.2. IO Types Notation

Signal	Description
1V8, 2V8 or 3V3	Digital Signal Voltage Level
Analog	Analog Signal
GND	Ground
Power	Power supply
VIN	Input Voltage

3.3. Pin-out Description

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
1	Power	VIN				Module power supply input (3.6V-5.5V)
2	Power	VIN				
3	Power	VIN				
4	Power	VIN				
5	Power	VIO				3.3V power supply output (up to 1A)
6	Power	VIO				
7	Power	VIO				
8	1V8	BOOT MODE	IMX_BOOT_MODE			Boot mode select L: Boot from NAND / H: Boot from UART/USB
9	Power	3V3				3.3V power supply output (up to 1A)
10	Power	3V3				
11	Power	3V3				
12	Power	3V3				
13	Power	VBACKUP				Supply voltage must be held between 2.6V and 3.1V for proper DA9053 operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature.
14	VIN	POWER_ON			100K-PU to VIN	ON/OFF key with optional long press shutdown. To power up/down, drive the POWER_ON pin LOW. Refer to DA9053 datasheet for nONKEY pin details.
15	3V3	#RESET_OUT	GPIO_17	ESAI1_TX0 SDMA_EXT_EVENT[0] GPC_PMIC_RDY RTC_CE_RTC_FSV_TRIG SPDIF_OUT1 SNOOP2 SJC_JTAG_ACT	GPIO7[12]	#RESET_OUT may be used to reset peripherals on the carrier board. This signal can be controller by a GPIO function during runtime

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
16	VIN	#POR	POR_B		10K-PU to VIN	Power On Reset—Active low input signal. Leave unconnected, if not used.
17	1V8	#RESET_IN	RESET_IN_B	RESET_B	10K-PU to 1V8	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module, SDRAMC module, and the clock control module) are reset.
18	GND	GND				
ETHERNET						
19	Analog	ETN_TXN				Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	3V3	ETN_LINK_LED				Active low - output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation.
21	Analog	ETN_TXP				Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	Power	ETN_VDD				+3.3V analog power supply output to magnetics
23	Analog	ETN_RXN				Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	3V3	ETN_ACT_LED				Active low - output is driven active whenever the device detects a valid link, and blinks indicating activity.
25	Analog	ETN_RXP				Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND				
USB HOST						
27	3V3	USBH_VBUS_EN	EIM_D31	WEIM_D[31] UART3_RTS CSI0_D[2] DI0_PIN12 DISP1_DAT[20] USBOH3_USBH1_PWR USBOH3_USBH2_PWR	GPIO3[31]	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
28	3V3	#USBH_OC	EIM_D30	WEIM_D[30] UART3_CTS CSI0_D[3] DI0_PIN11 DISP1_DAT[21] USBOH3_USBH1_OC USBOH3_USBH2_OC	GPIO3[30] 10K-PU	Active low over-current indicator input connected to a GPIO.
29	Analog	USBH_DM	USB_H1_DN			D- pin of the USB cable
30	Analog	USBH_VBUS	USB_H1_VBUS			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
31	Analog	USBH_DP	USB_H1_DP			D+ pin of the USB cable
32	GND	GND				
USB OTG/2nd CAN						
33	3V3	USBO_ID	USB_OTG_ID			ID pin of the USB cable. For an A-Device ID is grounded. For a B-device ID is floated.
34	3V3	USBO_VBUS_EN CAN_TX	GPIO_7	ESAI1_TX4_RX1 EPIT1_EPITO CAN1_TXCAN UART2_TXD FIRI_RXD SPDIF_PLOCK CCM_PLL2_BYP	**GPIO1[7]**	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
35	Analog	USBO_DM	USB_OTG_DN			D- pin of the USB cable
36	3V3	#USBO_OC CAN_RX	GPIO_8	ESAI1_TX5_RX0 EPIT2_EPITO CAN1_RXCAN UART2_RXD FIRI_TXD SPDIF_SRCLK CCM_PLL3_BYP	**GPIO1[8]** 10K-PU	Active low over-current indicator input connected to a GPIO.
37	Analog	USBO_DP	USB_OTG_DP			D+ pin of the USB cable
38	Analog	USBO_VBUS	USB_OTG_VBUS			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
39	GND	GND				
I2C INTERFACE						
40	3V3	I2C_DATA	GPIO_6	ESAI1_SCKT **I2C3_SDA** CCM_CCM_OUT_0 CSU_INT_DEB OBSRV_INT_OUT1 ESDHC2_LCTL MLBSIG	GPIO1[6] 10K-PU	I2C Data
41	3V3	I2C_CLK	GPIO_3	ESAI1_HCKR **I2C3_SCL** DPLLIP1_TOG_EN CCM_CLKO2 OBSRV_INT_OUT0 USBOH3_USBH1_OC MLBCLK	GPIO1[3] 10K-PU	I2C Clock
PWM INTERFACE						
42	3V3	PWM	GPIO_1	ESAI1_SCKR KPP_ROW[5] CCM_SSI_EXT2_CLK **PWM2_PWMO** WDOG2_WDOG_B ESDHC1_CD TESTER_ACK	GPIO1[1]	PWM Output
1 WIRE INTERFACE						
43	3V3	OWIRE	GPIO_18	ESAI1_TX1 SDMA_EXT_EVENT[1] **OWIRE_LINE** RTC_CE_RTC_ALARM2_T	GPIO7[13]	1-Wire bus. Requires an external pull-up resistor. The recommended resistor is specified by the generic 1-Wire device used in a given system.

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
				RIG CCM_ASRC_EXT_CLK ESDHC1_LCTL SYSTEM_RST		
CSPI – CONFIGURABLE SERIAL PERPHERAL INTERFACE						
44	3V3	CSPI_SS0	EIM_EB2	WEIM_EB[2] CCM_DI1_EXT_CLK SER_DISP1_CS **ECSPI1_SS0** I2C2_SCL	GPIO2[30]	Slave Select (Selectable polarity) signal
45	3V3	CSPI_SS1	EIM_D19	WEIM_D[19] DI0_PIN8 DISPB1_SER_RS **ECSPI1_SS1** EPIT1_EPITO UART1_CTS USBOH3_USBH2_OC	GPIO3[19]	Slave Select (Selectable polarity) signal
46	3V3	CSPI_MOSI	EIM_D18	WEIM_D[18] DI0_PIN7 DISPB1_SER_DIO **ECSPI1_MOSI** I2C3_SDA DI1_D0_CS	GPIO3[18]	Master Out/Slave In signal
47	3V3	CSPI_MISO	EIM_D17	ecspi1_MISOWEIM_D[17] DI0_PIN6 DISPB1_SER_DIN **ECSPI1_MISO** I2C3_SCL	GPIO3[17]	Master In/Slave Out signal
48	3V3	CSP_CLK	EIM_D16	WEIM_D[16] DI0_PIN5 DISPB1_SER_CLK **ECSPI1_SCLK** I2C2_SDA	GPIO3[16]	Serial Clock signal
49	3V3	CSPI_RDY	GPIO_19	KPP_COL[5] CCM_CLKO SPDIF_OUT1 RTC_CE_RTC_EXT_TRIG2 **ECSPI1_RDY** FEC_TDATA[3] INT_BOOT	GPIO4[5]	Serial Data Ready signal
50	GND	GND				
SD – SECURE DIGITAL INTERFACE 1						
51	3V3	SD1_CD	EIM_D24	WEIM_D[24] UART3_TXD ECSPI1_SS2 CSPI_SS2 AUD5_RXFS ECSPI2_SS2 UART1_DTR	**GPIO3[24]**	SD Card Detect – connected to a GPIO
52	3V3	SD1_D0	SD1_DATA0	**ESDHC1_DAT0** GPT_CAPIN1 CSPI_MISO CCM_PLL3_BYP	GPIO1[16]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
53	3V3	SD1_D1	SD1_DATA1	**ESDHC1_DAT1** GPT_CAPIN2 CSPI_SS0 CCM_PLL4_BYP	GPIO1[17]	

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
54	3V3	SD1_D2	SD1_DATA2	**ESDHC1_DAT2** GPT_CMPOUT2 PWM2_PWMO WDOG1_WDOG_B CSPI_SS1 CCM_PLL2_BYP	GPIO1[19]	
55	3V3	SD1_D3	SD1_DATA3	**ESDHC1_DAT3** GPT_CMPOUT3 PWM1_PWMO WDOG2_WDOG_B CSPI_SS2 SATA_PHY_DTB[1]	GPIO1[21]	
56	3V3	SD1_CMD	SD1_CMD	**ESDHC1_CMD** GPT_CMPOUT1 CSPI_MOSI CCM_PLL1_BYP	GPIO1[18]	SD Command (bidirectional signal)
57	3V3	SD1_CLK	SD1_CLK	**ESDHC1_CLK** OSC32K_32K_OUT GPT_CLKIN CSPI_SCLK SATA_PHY_DTB[0]	GPIO1[20]	SD Output Clock.
58	GND	GND				
1st UART						
59	3V3	UART1_TXD	PATA_DIOW	PATA_DIOW **UART1_TXD** USBPHY2_DATAOUT[2]	GPIO6[17]	Application UART 1 Transmit Data output signal
60	3V3	UART1_RXD	PATA_DMACK	PATA_DMACK **UART1_RXD** USBPHY2_DATAOUT[3]	GPIO6[18]	Application UART 1 Receive Data input signal
61	3V3	UART1_RTS	PATA_IORDY	PATA_IORDY ESDHC3_CLK **UART1_RTS** CAN2_RXCAN USBPHY1_DATAOUT[1]	GPIO7[5]	Application UART 1 Request to Send **input** signal
62	3V3	UART1_CTS	PATA_RESET_B	PATA_RESET_B ESDHC3_CMD **UART1_CTS** CAN2_TXCAN USBPHY1_DATAOUT[0]	GPIO7[4]	Application UART 1 Clear to Send **output** signal
2nd UART						
63	3V3	UART2_TXD	PATA_DMARQ	PATA_DMARQ **UART2_TXD** CCM_CCM_OUT_0 USBPHY2_DATAOUT[4]	GPIO7[0]	Application UART 2 Transmit Data output signal
64	3V3	UART2_RXD	PATA_BUFFER_EN	PATA_BUFFER_EN **UART2_RXD** CCM_CCM_OUT_1 USBPHY2_DATAOUT[5]	GPIO7[1]	Application UART 2 Receive Data input signal
65	3V3	UART2_RTS	PATA_DIOR	PATA_DIOR **UART2_RTS** CAN1_RXCAN USBPHY2_DATAOUT[7]	GPIO7[3]	Application UART 2 Request to Send **input** signal
66	3V3	UART2_CTS	PATA_INTRQ	PATA_INTRQ **UART2_CTS** CAN1_TXCAN CCM_CCM_OUT_2	GPIO7[2]	Application UART 2 Clear to Send **output** signal

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
				USBPHY2_DATAOUT[6]		
3rd UART						
67	3V3	UART3_TXD	PATA_CS_0	PATA_CS_0 **UART3_TXD** USBPHY1_DATAOUT[5]	GPIO7[9]	Application UART 3 Transmit Data output signal
68	3V3	UART3_RXD	PATA_CS_1	PATA_CS_1 **UART3_RXD** USBPHY1_DATAOUT[6]	GPIO7[10]	Application UART 3 Receive Data input signal
69	3V3	UART3_RTS	PATA_DA_2	PATA_DA_2 ESDHC4_CLK **UART3_RTS** USBPHY1_DATAOUT[4]	GPIO7[8]	Application UART 3 Request to Send **input** signal
70	3V3	UART3_CTS	PATA_DA_1	PATA_DA_1 ESDHC4_CMD **UART3_CTS** USBPHY1_DATAOUT[3]	GPIO7[7]	Application UART 3 Clear to Send **output** signal
71	GND	GND	GND		GND	
KEYPAD / 1st CAN						
72	3V3	KP_COL0	GPIO_9	ESAI1_FSR **KPP_COL[6]** CCM_REF_EN_B PWM1_PWMO WDOG1_WDOG_B ESDHC1_WP SCC_FAIL_STATE	GPIO1[9]	
73	3V3	KP_COL1	GPIO_4	ESAI1_HCKT **KPP_COL[7]** CCM_CCM_OUT_2 CSU_ALARM_AUT[1] OBSRV_INT_OUT3 ESDHC2_CD SCC_SEC_STATE	GPIO1[4]	
74	3V3	KP_COL2	KEY_COL2	**KPP_COL[2]** CAN1_TXCAN 32K_256K_CTI_TRIGOUT6 FEC_MDIO ECSPI1_SS1 FEC_RDATA[2] USBPHY1_RXACTIVE	GPIO4[10]	
75	3V3	KP_COL3	KEY_COL3	**KPP_COL[3]** USBOH3_H2_DP SPDIF_IN1 I2C2_SCL ECSPI1_SS3 FEC_CRS USBPHY1_SIECLOCK	GPIO4[12]	
76	3V3	KP_COL4 TXCAN	KEY_COL4	KPP_COL[4] **CAN2_TXCAN** SISG[4] UART5_RTS USBOH3_USBOTG_OC USBPHY1_LINESTATE[1]	GPIO4[14]	
77	3V3	KP_ROW0	GPIO_2	ESAI1_FST **KPP_ROW[6]** CCM_CCM_OUT_1 CSU_ALARM_AUT[0]	GPIO1[2]	

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
				OBSRV_INT_OUT2 ESDHC2_WP MLBDAT		
78	3V3	KP_ROW1	GPIO_5	ESAI1_TX2_RX3 **KPP_ROW[7]** CCM_CLKO CSU_ALARM_AUT[2] OBSRV_INT_OUT4 I2C3_SCL CCM_PLL1_BYP	GPIO1[5]	
79	3V3	KP_ROW2	KEY_ROW2	**KPP_ROW[2]** CAN1_RXCAN 32K_256K_CTI_TRIGOUT7 FEC_MDC ECSPI1_SS2 FEC_TDATA[2] USBPHY1_RXERROR	GPIO4[11]	
80	3V3	KP_ROW3	KEY_ROW3	**KPP_ROW[3]** USBOH3_H2_DM CCM_ASRC_EXT_CLK I2C2_SDA OSC32K_32K_OUT CCM_PLL4_BYP USBPHY1_LINESTATE[0]	GPIO4[13]	
81	3V3	KP_ROW4 RXCAN	KEY_ROW4	KPP_ROW[4] **CAN2_RXCAN** SISG[5] UART5_CTS USBOH3_USBOTG_PWR USBPHY1_VBUSVALID	GPIO4[15]	
82	GND	GND				
SSI 1 - Serial Audio Port 1						
83	3V3	SSI1_INT	EIM_D26	WEIM_D[26] UART2_TXD FIRI_RXD CSI0_D[1] DI1_PIN11 SISG[2] DISP1_DAT[22]	**GPIO3[26]**	GPIO
84	3V3	SSI1_RXD	KEY_ROW1	KPP_ROW[1] **AUD5_RXD** 32K_256K_CTI_TRIGOUT_ACK7 UART5_RXD ECSPI1_SS0 FEC_COL USBPHY1_RXVALID	GPIO4[9]	Serial Audio Interface serial data line 1
85	3V3	SSI1_TXD	KEY_ROW0	KPP_ROW[0] **AUD5_TXD** 32K_256K_CTI_TRIGIN_ACK7 UART4_RXD ECSPI1_MOSI FEC_TX_ER	GPIO4[7]	Serial Audio Interface serial data line 0
86	3V3	SSI1_CLK	KEY_COL0	KPP_COL[0] **AUD5_TXC** 32K_256K_CTI_TRIGIN7 UART4_TXD	GPIO4[6]	Serial Audio Interface serial bit clock

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
				ECSPI1_SCLK FEC_RDATA[3] ANY_PU_RST		
87	3V3	SSI1_FS	KEY_COL1	KPP_COL[1] **AUD5_TXFS** 32K_256K_CTI_TRIGOUT_ACK6 UART5_TXD ECSPI1_MISO FEC_RX_CLK USBPHY1_TXREADY	GPIO4[8]	Serial Audio Interface left/right clock
88	GND	GND				
SSI 2 - Serial Audio Port 2						
89	3V3	SSI2_INT	EIM_D27	WEIM_D[27] UART2_RXD FIRI_TXD CSI0_D[0] DI1_PIN13 SISG[3] DISP1_DAT[23]	**GPIO3[27]**	GPIO
90	3V3	SSI2_RXD	CSI0_DAT7	CSI0_D[7] KPP_ROW[6] ECSPI1_SS0 USBOH3_USBH3_DIR **AUD3_RXD**	GPIO5[25]	Serial Audio Interface serial data line 1
91	3V3	SSI2_TXD	CSI0_DAT5	CSI0_D[5] KPP_ROW[5] ECSPI1_MOSI USBOH3_USBH3_NXT **AUD3_TXD**	GPIO5[23]	Serial Audio Interface serial data line 0
92	3V3	SSI2_CLK	CSI0_DAT4	CSI0_D[4] KPP_COL[5] ECSPI1_SCLK USBOH3_USBH3_STP **AUD3_TXC**	GPIO5[22]	Serial Audio Interface serial bit clock
93	3V3	SSI2_FS	CSI0_DAT6	CSI0_D[6] KPP_COL[6] ECSPI1_MISO USBOH3_USBH3_CLK **AUD3_TXFS**	GPIO5[24]	Frame Sync
94	GND	GND				
SD – SECURE DIGITAL INTERFACE 2						
95	3V3	SD2_CD	EIM_D25	WEIM_D[25] UART3_RXD ECSPI1_SS3 CSPI_SS3 AUD5_RXC ECSPI2_SS3 UART1_DSR	GPIO3[25]	SD Card Detect – connected to a GPIO
96	3V3	SD2_D0	SD2_DATA0	**ESDHC2_DAT0** KPP_ROW[7] AUD4_RXD CSPI_MISO RTIC_RTIC_DONE_INT	GPIO1[15]	SD Data (bidirectional signal) - If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added
97	3V3	SD2_D1	SD2_DATA1	**ESDHC2_DAT1** KPP_COL[7]	GPIO1[14]	

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
				AUD4_TXFS CSPI_SS0 RTIC_RTIC_SEC_VIO		
98	3V3	SD2_D2	SD2_DATA2	**ESDHC2_DAT2** KPP_ROW[6] AUD4_TXD CSPI_SS1 SJC_FAIL	GPIO1[13]	
99	3V3	SD2_D3	SD2_DATA3	**ESDHC2_DAT3** KPP_COL[6] AUD4_TXC CSPI_SS2 SJC_DONE	GPIO1[12]	
100	3V3	SD2_CMD	SD2_CMD	**ESDHC2_CMD** KPP_ROW[5] AUD4_RXC CSPI_MOSI SCC_RANDOM	GPIO1[11]	SD command bidirectional signal
101	3V3	SD2 CLK	SD2_CLK	**ESDHC2_CLK** KPP_COL[5] AUD4_RXFS CSPI_SCLK SCC_RANDOM_V	GPIO1[10]	SD Output Clock
102	GND	GND				
CMOS SENSOR INTERFACE						
103	3V3	CSI_D0	CSI0_DAT12	**CSI0_D[12]** UART4_TXD USBOH3_USBH3_DATA[0]	GPIO5[30]	
104	3V3	CSI_D1	CSI0_DAT13	**CSI0_D[13]** UART4_RXD USBOH3_USBH3_DATA[1]	GPIO5[31]	
105	3V3	CSI_D2	CSI0_DAT14	**CSI0_D[14]** UART5_TXD USBOH3_USBH3_DATA[2]	GPIO6[0]	
106	3V3	CSI_D3	CSI0_DAT15	**CSI0_D[15]** UART5_RXD USBOH3_USBH3_DATA[3]	GPIO6[1]	
107	3V3	CSI_D4	CSI0_DAT16	**CSI0_D[16]** UART4_RTS USBOH3_USBH3_DATA[4]	GPIO6[2]	
108	3V3	CSI_D5	CSI0_DAT17	**CSI0_D[17]** UART4_CTS USBOH3_USBH3_DATA[5]	GPIO6[3]	
109	3V3	CSI_D6	CSI0_DAT18	**CSI0_D[18]** UART5_RTS USBOH3_USBH3_DATA[6]	GPIO6[4]	
110	3V3	CSI_D7	CSI0_DAT19	**CSI0_D[19]** UART5_CTS USBOH3_USBH3_DATA[7] USBPHY2_BISTOK	GPIO6[5]	
111	GND	GND				
112	3V3	CSI_HSYNC	CSI0_MCLK	**CSI0_HSYNC** CCM_CSI0_MCLK	GPIO5[19]	
113	3V3	CSI_VSYNC	CSI0_VSYNC	**CSI0_VSYNC**	GPIO5[21]	

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
114	3V3	CSI_PIXCLK	CSI0_PIXCLK	**CSI0_PIXCLK**	GPIO5[18]	
115	3V3	CSI_MCLK	GPIO_0	**CCM_CLKO** KPP_COL[5] CCM_SSI_EXT1_CLK EPIT1_EPITO SRTC_ALARM_DEB USBOH3_USBH1_PWR TD	GPIO1[0]	
116	GND	GND				
LCD Controller and Smart LCD Controller						
117	2V8	LCD_D0	DISP0_DAT0	**DISP0_DAT[0]** CSPI_SCLK USBOH3_USBH2_DATA[0] USBPHY2_TXREADY	GPIO4[21]	LCD Data Bus
118	2V8	LCD_D1	DISP0_DAT1	**DISP0_DAT[1]** CSPI_MOSI USBOH3_USBH2_DATA[1] USBPHY2_RXVALID	GPIO4[22]	LCD Data Bus
119	2V8	LCD_D2	DISP0_DAT2	**DISP0_DAT[2]** CSPI_MISO USBOH3_USBH2_DATA[2] USBPHY2_RXACTIVE	GPIO4[23]	LCD Data Bus
120	2V8	LCD_D3	DISP0_DAT3	**DISP0_DAT[3]** CSPI_SS0 USBOH3_USBH2_DATA[3] USBPHY2_RXERROR	GPIO4[24]	LCD Data Bus
121	2V8	LCD_D4	DISP0_DAT4	**DISP0_DAT[4]** CSPI_SS1 USBOH3_USBH2_DATA[4] USBPHY2_SIECLOCK	GPIO4[25]	LCD Data Bus
122	2V8	LCD_D5	DISP0_DAT5	**DISP0_DAT[5]** CSPI_SS2 USBOH3_USBH2_DATA[5] USBPHY2_LINESTATE[0]	GPIO4[26]	LCD Data Bus
123	2V8	LCD_D6	DISP0_DAT6	**DISP0_DAT[6]** CSPI_SS3 USBOH3_USBH2_DATA[6] USBPHY2_LINESTATE[1]	GPIO4[27]	LCD Data Bus
124	2V8	LCD_D7	DISP0_DAT7	**DISP0_DAT[7]** CSPI_RDY USBOH3_USBH2_DATA[7] USBPHY2_VBUSVALID	GPIO4[28]	LCD Data Bus
125	2V8	LCD_D8	DISP0_DAT8	**DISP0_DAT[8]** PWM1_PWMO WDOG1_WDOG_B USBPHY2_AVALID	GPIO4[29]	LCD Data Bus
126	2V8	LCD_D9	DISP0_DAT9	**DISP0_DAT[9]** PWM2_PWMO WDOG2_WDOG_B USBPHY2_VSTATUS[0]	GPIO4[30]	LCD Data Bus
127	2V8	LCD_D10	DISP0_DAT10	**DISP0_DAT[10]** USBOH3_USBH2_STP USBPHY2_VSTATUS[1]	GPIO4[31]	LCD Data Bus
128	2V8	LCD_D11	DISP0_DAT11	**DISP0_DAT[11]** USBOH3_USBH2_NXT USBPHY2_VSTATUS[2]	GPIO5[5]	LCD Data Bus

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
129	GND	GND				
130	2V8	LCD_D12	DISP0_DAT12	**DISP0_DAT[12]** USBOH3_USBH2_CLK USBPHY2_VSTATUS[3]	GPIO5[6]	LCD Data Bus
131	2V8	LCD_D13	DISP0_DAT13	**DISP0_DAT[13]** AUD5_RXFS USBPHY2_VSTATUS[4]	GPIO5[7]	LCD Data Bus
132	2V8	LCD_D14	DISP0_DAT14	**DISP0_DAT[14]** AUD5_RXC USBPHY2_VSTATUS[5]	GPIO5[8]	LCD Data Bus
133	2V8	LCD_D15	DISP0_DAT15	**DISP0_DAT[15]** ECSPI1_SS1 ECSPI2_SS1 USBPHY2_VSTATUS[6]	GPIO5[9]	LCD Data Bus
134	2V8	LCD_D16	DISP0_DAT16	**DISP0_DAT[16]** ECSPI2_MOSI AUD5_TXC SDMA_EXT_EVENT[0] USBPHY2_VSTATUS[7]	GPIO5[10]	LCD Data Bus
135	2V8	LCD_D17	DISP0_DAT17	**DISP0_DAT[17]** ECSPI2_MISO AUD5_TXD SDMA_EXT_EVENT[1]	GPIO5[11]	LCD Data Bus
136	2V8	LCD_D18	DISP0_DAT18	**DISP0_DAT[18]** ECSPI2_SS0 AUD5_TXFS AUD4_RXFS WEIM_CS[2]	GPIO5[12]	LCD Data Bus
137	2V8	LCD_D19	DISP0_DAT19	**DISP0_DAT[19]** ECSPI2_SCLK AUD5_RXD AUD4_RXC WEIM_CS[3]	GPIO5[13]	LCD Data Bus
138	2V8	LCD_D20	DISP0_DAT20	**DISP0_DAT[20]** ECSPI1_SCLK AUD4_TXC	GPIO5[14]	LCD Data Bus
139	2V8	LCD_D21	DISP0_DAT21	**DISP0_DAT[21]** ECSPI1_MOSI AUD4_TXD	GPIO5[15]	LCD Data Bus
140	2V8	LCD_D22	DISP0_DAT22	**DISP0_DAT[22]** ECSPI1_MISO AUD4_TXFS	GPIO5[16]	LCD Data Bus
141	2V8	LCD_D23	DISP0_DAT23	**DISP0_DAT[23]** ECSPI1_SS0 AUD4_RXD	GPIO5[17]	LCD Data Bus
142	GND	GND				
143	2V8	LCD_HSYNC	DI0_PIN2	**DI0_PIN2** AUD6_TXD USBPHY1_ENDSESSION	GPIO4[18]	
144	2V8	LCD_VSYNC	DI0_PIN3	**DI0_PIN3** AUD6_TXFS USBPHY1_IDDIG	GPIO4[19]	
145	2V8	LCD_OE_ACD	DI0_PIN15	**DI0_PIN15** AUD6_TXC	GPIO4[17]	

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
				USBPHY1_BVALID		
146	2V8	LCD_SCLK	DI0_DISP_CLK	**DI0_DISP_CLK** USBOH3_USBH2_DIR USBPHY1_AVALID	GPIO4[16]	
147	GND	GND				
MODULE SPECIFIC SIGNALS						
148	3V3	CSI1_MCLK	NANDF_CS2	NANDF_CS[2] SISG[0] / ESAI1_TX0 WEIM_CRE CCM_CSI0_MCLK MLBSIG USBPHY1_VSTATUS[6]	GPIO6[15]	
149	3V3	CSI1_PIXCLK	EIM_A16	esdhc1_WPWEIM_A[16] DI1_DISP_CLK CSI1_PIXCLK BT_CFG1[1]	GPIO2[22]	
150	3V3	CSI1_VSYNC	EIM_D29	gpio2_GPIO[4]WEIM_D[29] UART2_RTS DISPB0_SER_RS CSPI_SS0 / DI1_PIN15 CSI1_VSYNC DI0_PIN14	GPIO3[29]	
151	3V3	CSI1_HSYNC	EIM_EB3	WEIM_EB[3] UART3_RTS UART1_RI / DI1_PIN3 CSI1_HSYNC DI1_PIN16	GPIO2[31]	
152	3V3	CSI1_D12	EIM_A17	WEIM_A[17] DISP1_DAT[12] CSI1_D[12] BT_CFG1[2]	GPIO2[21]	
153	3V3	CSI1_D13	EIM_A18	WEIM_A[18] DISP1_DAT[13] CSI1_D[13] BT_CFG1[3]	GPIO2[20]	
154	3V3	CSI1_D14	EIM_A19	WEIM_A[19] DISP1_DAT[14] CSI1_D[14] BT_CFG1[4]	GPIO2[19]	
155	3V3	CSI1_D15	EIM_A20	WEIM_A[20] DISP1_DAT[15] CSI1_D[15] BT_CFG1[5]	GPIO2[18]	
156	3V3	CSI1_D16	EIM_A21	WEIM_A[21] DISP1_DAT[16] CSI1_D[16] BT_CFG1[6]	GPIO2[17]	
157	3V3	CSI1_D17	EIM_A22	WEIM_A[22] DISP1_DAT[17] CSI1_D[17] BT_CFG1[7]	GPIO2[16]	
158	3V3	CSI1_D18	EIM_A23	WEIM_A[23] DISP1_DAT[18] CSI1_D[18] / SISG[3] USBPHY2_ENDSESSION	GPIO6[6]	

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
159	3V3	CSI1_D19	EIM_A24	WEIM_A[24] DISP1_DAT[19] CSI1_D[19] / SISG[2] USBPHY2_BVALID	GPIO5[4]	
160	GND	GND				
161	3V3		CSI0_DAT8	CSI0_D[8] / KPP_COL[7] ECSPI2_SCLK USBOH3_USBH3_OC I2C1_SDA	GPIO5[26]	
162	3V3		CSI0_DAT9	CSI0_D[9] / KPP_ROW[7] ECSPI2_MOSI USBOH3_USBH3_PWR I2C1_SCL	GPIO5[27]	
163	3V3		CSI0_DAT10	CSI0_D[10] UART1_TXD ECSPI2_MISO AUD3_RXC	GPIO5[28]	
164	3V3		CSI0_DAT11	CSI0_D[11] UART1_RXD ECSPI2_SS0 AUD3_RXFS	GPIO5[29]	
165	3V3		EIM_D22	WEIM_D[22] DI0_PIN1 DISPB0_SER_DIN CSPI_MISO USBOH3_USBOTG_PWR	GPIO3[22]	
166	3V3		EIM_D23	WEIM_D[23] UART3_CTS UART1_DCD DI0_D0_CS DI1_PIN2 CSI1_DATA_EN DI1_PIN14	GPIO3[23]	
167	3V3	CKIH1	CKIH1			
168	3V3	TVDAC_IOB	TVDAC_IOB			
169	3V3	TVDAC_IOG	TVDAC_IOG			
170	3V3	TVDAC_IOR	TVDAC_IOR			
171	GND	GND				
172	3V3		GPIO_14		GPIO4[3]	GPIO_13 is used to signal PMIC nVDD_FAULT
173	3V3	EIM_CS0	EIM_CS0	WEIM_CS[0] ECSPI2_SCLK DI1_PIN5	GPIO2[23]	
174	3V3	EIM_CS1	EIM_CS1	WEIM_CS[1] ECSPI2_MOSI DI1_PIN6	GPIO2[24]	
175	3V3	GPIO	CSI0_DATA_EN	CSI0_DATA_EN	GPIO5[20]	EIM_DTACK is used on the i.MX51 processor, this function is not supported by the i.MX53 processor
176	3V3	EIM_WAIT	EIM_WAIT	WEIM_WAIT WEIM_DTACK_B	GPIO5[0]	
177	3V3	EIM_EB0	EIM_EB0	WEIM_EB[0] DISP1_DAT[11]	GPIO2[28]	

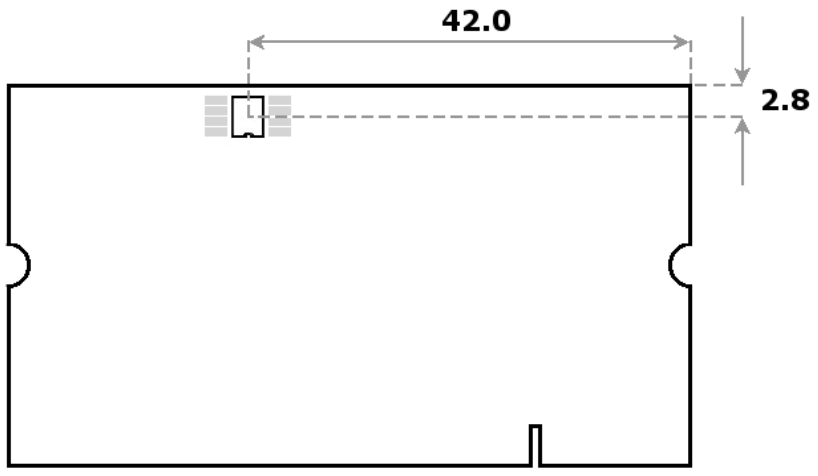
Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
				CSI1_D[11] GPC_PMIC_RDY BT_CFG2[7]		
178	3V3	EIM_EB1	EIM_EB1	WEIM_EB[1] DISP1_DAT[10] CSI1_D[10] BT_CFG2[6]	GPIO2[29]	
179	3V3	EIM_OE	EIM_OE	WEIM_OE ECSPI2_MISO DI1_PIN7 USBPHY2_IDDIG	GPIO2[25]	
180	3V3	EIM_LBA	EIM_LBA	WEIM_LBA ECSPI2_SS1 DI1_PIN17 BT_CFG1[0]	GPIO2[27]	
181	3V3	EIM_RW	EIM_RW	WEIM_RW ECSPI2_SS0 DI1_PIN8 USBPHY2_ HOSTDISCONNECT	GPIO2[26]	
182	3V3	EIM_BCLK	EIM_BCLK	WEIM_BCLK		
183	GND	GND				
184	3V3	EIM_DA0	EIM_DA0	NAND_WEIM_DA[0] DISP1_DAT[9] CSI1_D[9] / BT_CFG2[5]	GPIO3[0]	
185	3V3	EIM_DA1	EIM_DA1	NAND_WEIM_DA[1] DISP1_DAT[8] CSI1_D[8] / BT_CFG2[4]	GPIO3[1]	
186	3V3	EIM_DA2	EIM_DA2	NAND_WEIM_DA[2] DISP1_DAT[7] CSI1_D[7] / BT_CFG2[3]	GPIO3[2]	
187	3V3	EIM_DA3	EIM_DA3	NAND_WEIM_DA[3] DISP1_DAT[6] CSI1_D[6] / BT_CFG2[2]	GPIO3[3]	
188	3V3	EIM_DA4	EIM_DA4	NAND_WEIM_DA[4] DISP1_DAT[5] CSI1_D[5] / BT_CFG3[7]	GPIO3[4]	
189	3V3	EIM_DA5	EIM_DA5	NAND_WEIM_DA[5] DISP1_DAT[4] CSI1_D[4] / BT_CFG3[6]	GPIO3[5]	
190	3V3	EIM_DA6	EIM_DA6	NAND_WEIM_DA[6] DISP1_DAT[3] CSI1_D[3] / BT_CFG3[5]	GPIO3[6]	
191	3V3	EIM_DA7	EIM_DA7	NAND_WEIM_DA[7] DISP1_DAT[2] CSI1_D[2] / BT_CFG3[4]	GPIO3[7]	
192	3V3	EIM_DA8	EIM_DA8	NAND_WEIM_DA[8] DISP1_DAT[1] CSI1_D[1] / BT_CFG3[3]	GPIO3[8]	
193	3V3	EIM_DA9	EIM_DA9	NAND_WEIM_DA[9] DISP1_DAT[0] CSI1_D[0] / BT_CFG3[2]	GPIO3[9]	
194	3V3	EIM_DA10	EIM_DA10	NAND_WEIM_DA[10] DI1_PIN15	GPIO3[10]	

Pin	Type	Function	i.MX53 Pad Name	Alternate Functions		Description
				CSI1_DATA_EN BT_CFG3[1]		
195	3V3	EIM_DA11	EIM_DA11	NAND_WEIM_DA[11] DI1_PIN2 / CSI1_HSYNC	GPIO3[11]	
196	3V3	EIM_DA12	EIM_DA12	NAND_WEIM_DA[12] DI1_PIN3 CSI1_VSYNC	GPIO3[12]	
197	3V3	EIM_DA13	EIM_DA13	NAND_WEIM_DA[13] DI1_D0_CS CCM_DI1_EXT_CLK	GPIO3[13]	
198	3V3	EIM_DA14	EIM_DA14	NAND_WEIM_DA[14] DI1_D1_CS CCM_DI0_EXT_CLK	GPIO3[14]	
199	3V3	EIM_DA15	EIM_DA15	NAND_WEIM_DA[15] DI1_PIN1 DI1_PIN4	GPIO3[15]	
200	GND					

4. Voipac i.MX53 SODIMM module Connectors

4.1. Physical Locations

Along with the main 200pin SODIMM connector the Voipac i.MX53 SODIMM Module is equipped with pads for board-to-board pitch compression JTAG connector. The position is shown in the figure below.



Dimensions **(in millimeters)**

4.2. JTAG

Connector: Molex 47041-0001 www.molex.com

Pin#	Pin Name	Type	Description
1	+1V8	PWR	JTAG interface I/O voltage detect
2	GND	PWR	Ground
3	TMS	IN	JTAG mode select
4	nTRST	IN	JTAG reset
5	TCK	IN	JTAG clock
6	TDO	OUT	JTAG Data output
7	TDI	IN	JTAG Data input
8	nSRST	OUT	System reset

5. Technical Specifications

5.1. Electrical - Power Consumption

Table Part 1

VMX53 MAX				
Parameter	VIN	VIO	3V3	
	Pin	Pout	Pout	Pmod
State	[mW]	[mW]	[mW]	[mW]
Barebox	3271.41	-211.2	-82.75	2977.46
Linux	1212.75	-3.31	-72.82	1136.62
Memtest	2422.65	-3.3	-72.6	2346.75

Table Part 2

VMX53 MAX									
Test Point	TP100	TP100-101		TP103	TP102-103		TP105	TP104-105	
	U	U	I	U	U	I	U	U	I
State	[V]	[mV]	[mA]	[V]	[mV]	[mA]	[V]	[mV]	[mA]
Barebox	4.89	66.9	669	3.3	-6.4	-64	3.31	-2.5	-25
Linux	4.95	24.5	245	3.31	-0.1	-1	3.31	-2.2	-22
Memtest	4.65	52.1	521	3.3	-0.1	-1	3.3	-2.2	-22

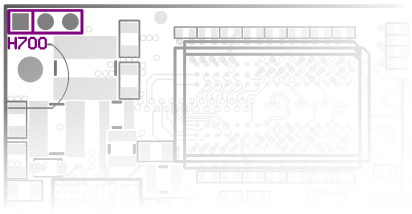
5.2. Electrical – DC Characteristics

See i.MX53 CPU datasheet at the Voipac Support CD in folder:
X:\Development Kit iMX53\SODIMM MODULE\doc\Components\iMX53

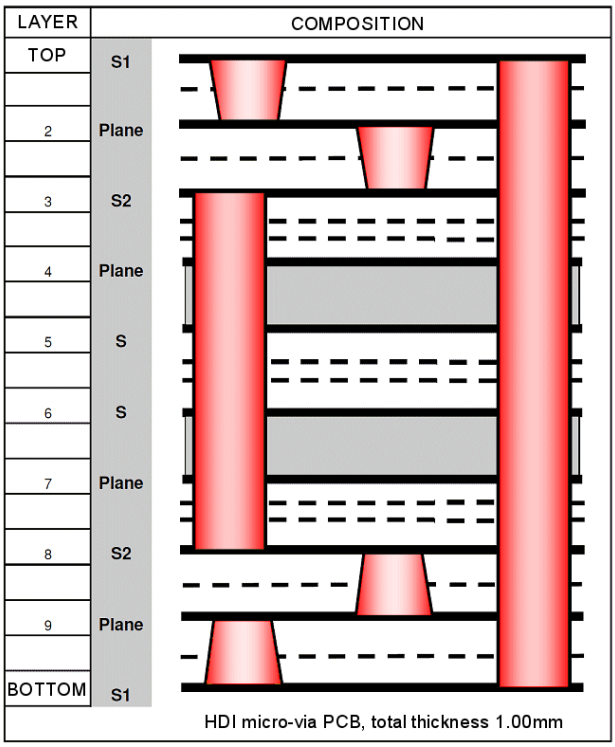
5.3. Electrical – Battery Power

Connector H700 (Upper left corner of the Module) enables battery power.

Pin#	Type	Description
1	VBAT	Main battery connection (max. 4.4V)
2	GND	Ground
3	TBAT	Connection to battery NTC resistor

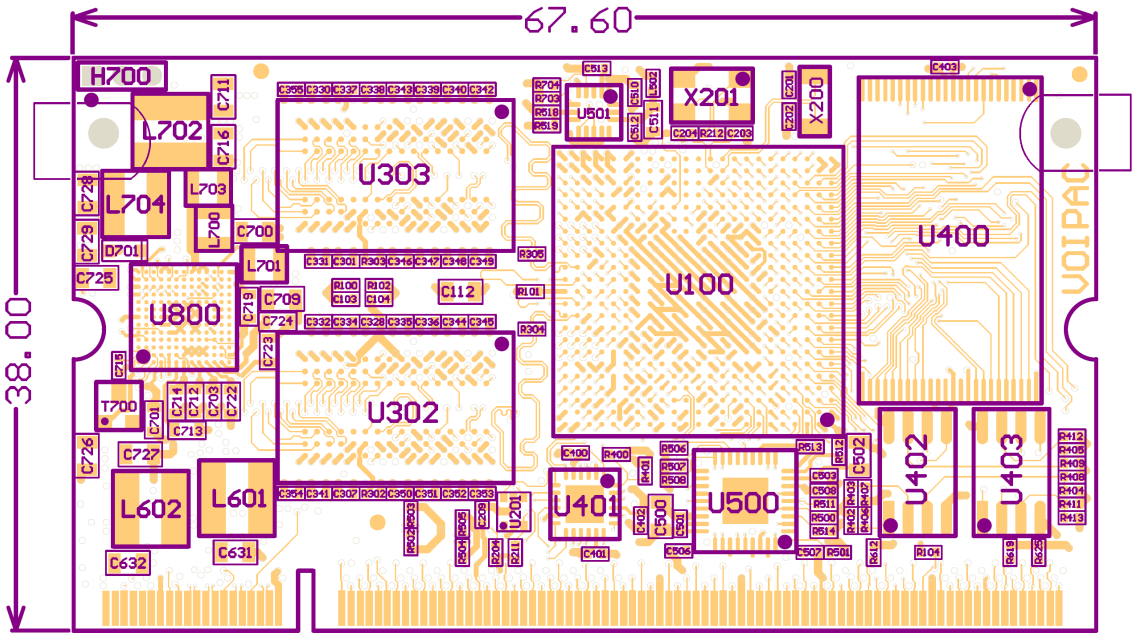


5.4. PCB Layer Structure

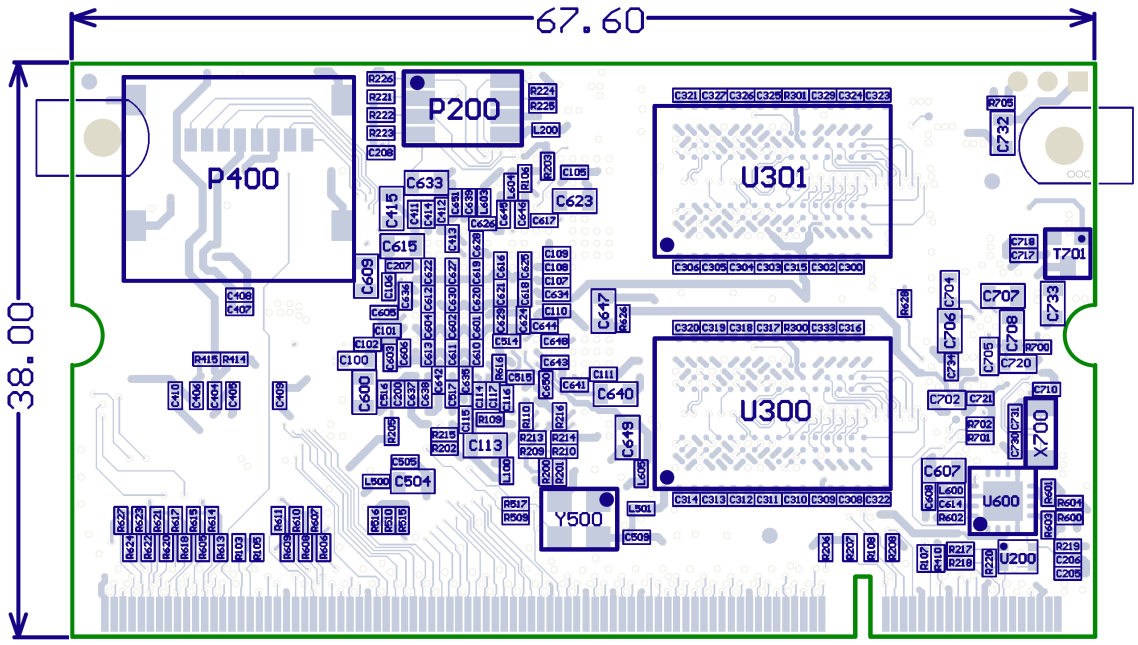


5.5. Mechanical

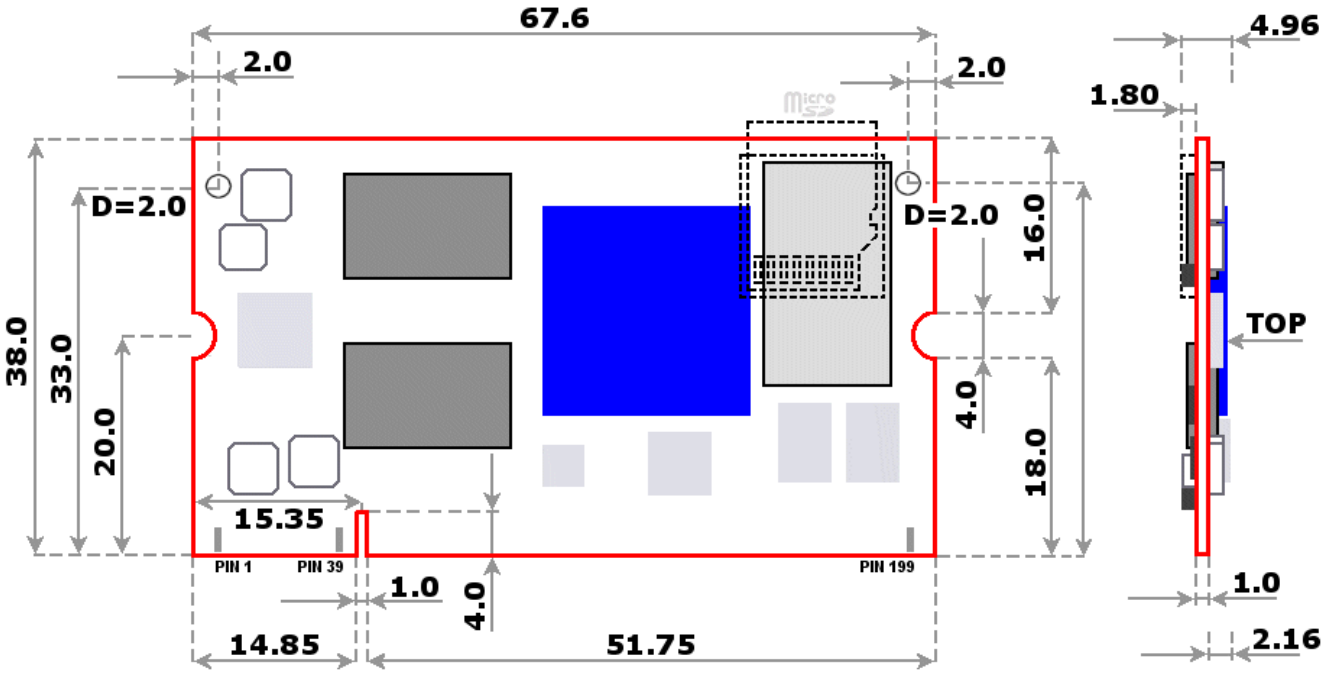
Top Layer **(in millimeters)**



Bottom Layer **(in millimeters)**



Dimensions **(in millimeters)**



5.6. Socket for the Voipac i.MX53 SODIMM module

The Voipac i.MX53 SODIMM Module fits into a regular 2.5V DDR1 SODIMM memory socket. More details are available in Manufacturer`s Datasheet or 3D View.

5.7. Temperature Range

Symbol	Description	Min	Max	Unit	Standard Unit Range
T_AMB	Operating temperature range - COMMERCIAL	0	+70	°C	
T_AMB	Operating temperature range - EXTENDED	-20	+70	°C	X
T_AMB	Operating temperature range - INDUSTRIAL*	-40	+85	°C	

* excluding microSD socket

5.8. RoHS and WEEE Compliance

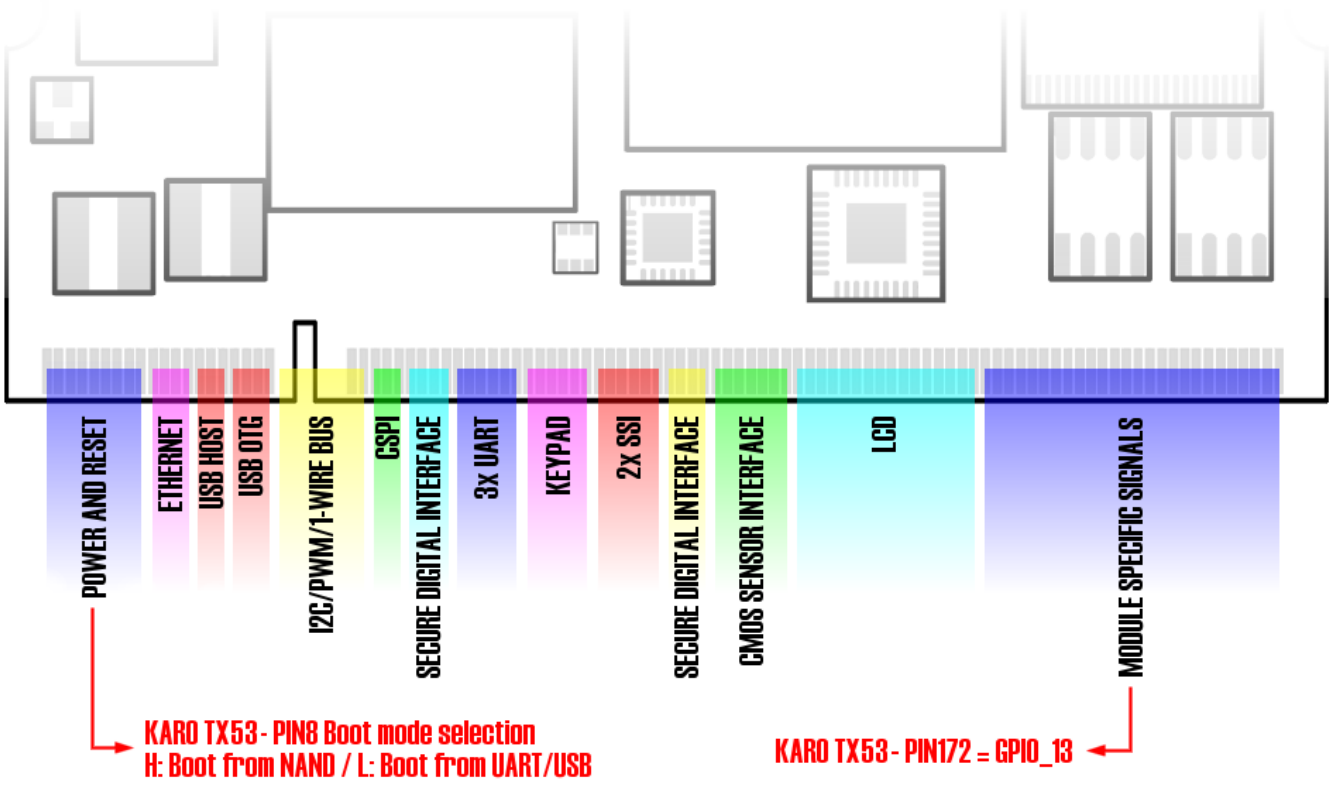
All of the products designed and manufactured by VOIPAC TECHNOLOGIES a.s. are classified as Electrical and Electronic Equipment (EEE) under the Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment 2002/95/EC (RoHS). To comply with the RoHS directive, the restricted use of Lead (Pb), Mercury (Hg), Cadmium (Cd), Hexavalent Chromium (Cr 6+), Polybrominated Biphenyls (PBB) and Polybrominated Diphenyl Ethers (PBDE) must be ensured. VOIPAC TECHNOLOGIES a.s. guarantees that products ordered after July 1, 2006 are assembled in full compliance with the RoHS directive from the European Parliament and Counsel. The company procedures also complies with the Waste Electrical and Electronic Equipment Directive 2002/96/EC (WEEE) .

6. Compatibility

Voipac i.MX53 SODIMM Module can be used as a replacement for Ka-Ro electronics TX53 Module. This chapter points out the differences for a smooth transition.

6.1. Ka-Ro electronics TX53 Module

Voipac i.MX53 SODIMM Module and TX53 from KaRo share the same pin mapping of all SODIMM pins, besides the General Purpose IOs and Module specific signals that may differ. For more details, see the picture below.



7. Support

All the relevant communication should be executed via e-mails preferably. Response time is up to 48 hours, except state holidays and weekends. VOIPAC TECHNOLOGIES a.s. Working hours are: 8:00 - 17:00, Monday – Friday.

To claim warranty and RMA number assignment, please fill in this protocol/problem description form and send it to: reclamations@voipac.com.
Board warranty claims without the protocol/problem description will not be processed.
For more information, see our General Terms and Conditions.

Besides the free-of-charge support, we provide support for your new designs when it comes to the special drivers for the peripherals not included in the Voipac development kits, design of your own base boards, prototyping, or even new products development, please contact: support@voipac.com for more info.

By registering on Voipac`s site, you will be granted to access the Voipac Ticketing System, where you can post support request tickets and receive e-mail notifications upon any change of your ticket's status.

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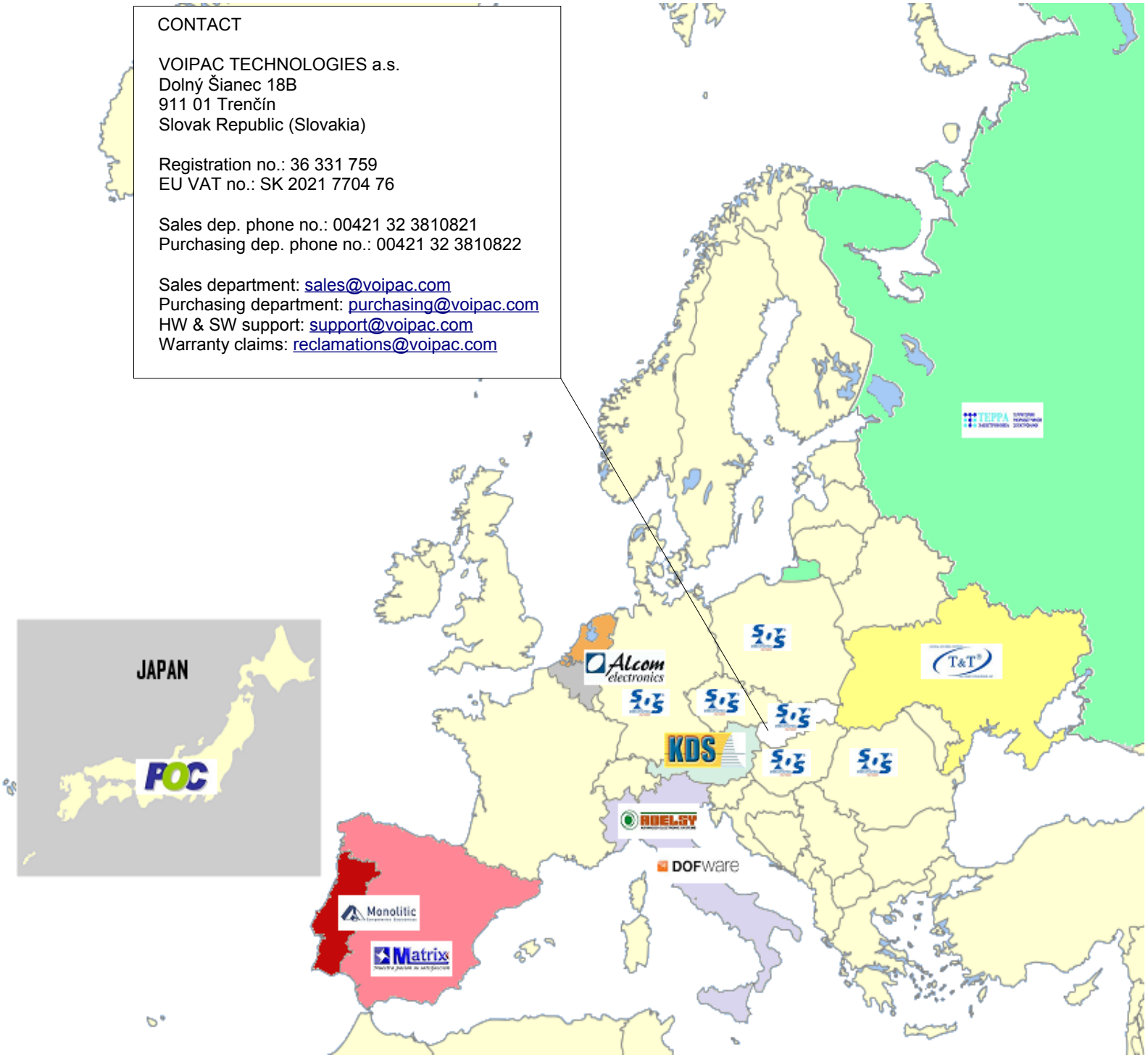
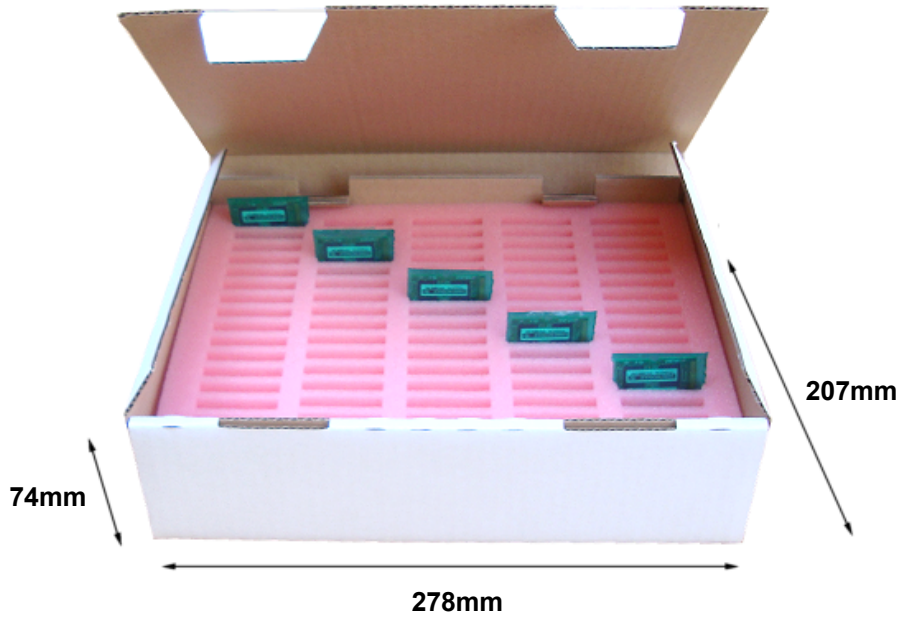


9. Ordering Information



The standard box includes 75pcs of modules, each of them sealed in ESD plastic bag.

Warranty:

VOIPAC TECHNOLOGIES a.s. Does Not Bear Responsibility for the Following:

- Failure of a product resulting from misuse, accident, modification, unsuitable operating environment, or improper maintenance by user
- Unless otherwise agreed in written, a product does not include technical support and the customer may be able to purchase technical support under separate agreement
- Any technical or other support provided under warranty by VOIPAC TECHNOLOGIES a.s. such as assistance, set-up and installation is provided WITHOUT WARRANTY OF ANY KIND.

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