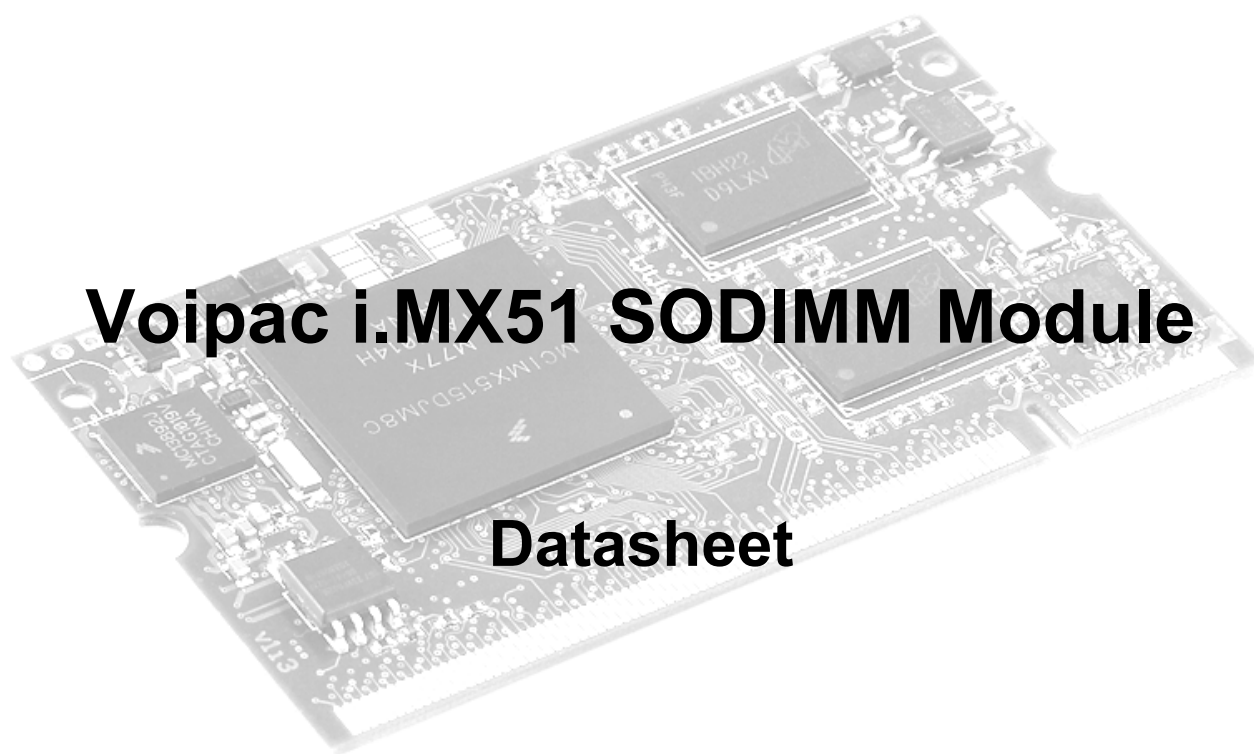




Date	Revision	Changes
15. March 2011	1.0	Initial Release
2. August 2011	1.1	Added Chapter 2.2: Features Modified Pin-out Description Table in Chapter 3.3 Modified Power Consumption Table in Chapter 5.1 Modified DC Characteristics Table in Chapter 5.2 Modified Temperature Range Table in Chapter 5.6

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1. Introduction

1.1. Hardware

The i.MX51 based module represents optimal performance and cost-effective solution for embedded systems. With preinstalled operating system and running up to 800MHz, the module enables almost anyone to design new product with quick set-up and easy-to-handle programming of own applications.

The i.MX51 SODIMM Module is a small circuit board which belongs to the group of COMs (Computer On Module). Its central component is the high-performance and low power consumption i.MX51 multimedia processor from Freescale™. This 1mm thick 10-layer microcontroller board includes all of the technologically and development demanding parts such as the CPU, Flash, SDRAM, I2C and Ethernet chip, saving many man-months of the high-frequency PCB design, complex prototyping, debugging and OS porting, thus minimizing the time-to-market of the customers' own applications.

The i.MX51 SODIMM format 200pin Module is available in 3 standard hardware configurations: BASIC / PROfesional / MAXimum. Upon request, any other possible configuration can be manufactured for no surcharge, minimum batch size is 10pcs. The operating temperature range of a standard unit is -20 / 70°C. Upon request, the module is available in -40 / 85°C operating temperature range for a surcharge. The standard i.MX51 SODIMM Module is equipped by i.MX515 ARM Cortex A8™ CPU, thus supporting all of the available CPU features.

The i.MX51 CPU is targeted at the automotive as well as the general embedded industrial markets, such as: terminals, automation, net applications, attendance systems, point of sales, gaming machines, navigations, netbooks and multimedia systems, building automation, security and surveillance systems, autopilots, handheld PCs, and many other fields, where there is a benefit of using operating system.

The i.MX51 belongs to the group of CPUs included in the [Freescale Product Longevity Program](#), that guarantees a minimum availability period of 15 years for the automotive and medical segments, and 10 years for all other market segments.

1.2. Software

Various operating systems are available for the Voipac i.MX51 SODIMM module provided by Voipac and the third parties. In case of unsupported operating system, necessary documentation for all hardware peripherals is freely available.

Voipac fully supports Linux operating system with drivers for all basic interfaces. Custom additional drivers for specific applications can be developed upon request.

Operating system	Description
Linux	Linux 2.6 with drivers for most common interfaces
Android	Android Gingerbread 2.3 (UNDER DEVELOPMENT)
Windows CE	Windows CE 6.0 (UNDER DEVELOPMENT)

1.3. Features Summary

Feature	Description
CPU	i.MX515 (Freescale) up to 800 MHz, ARM Cortex-A8™ CPU
DDR2 SDRAM	Up to 512MB
NAND FLASH	Up to 1GB
I2C EEPROM	Up to 1MB
LCD	LCD controller supporting WXVGA 1280x768px
AUDIO/TOUCH	Digital Audio IN/OUT, 4-wire touch controller
VIDEO CAPTURE	Still-Picture camera interface
VIDEO	HD Video encoder/decoder
MULTIMEDIA	• VPU – Video Processing Unit • IPU – Image Processing Unit • GPU 3D – OpenGL ES 2.0 • GPU 2D – OpenVG 1.1
ETHERNET	LAN8700 10/100Mbps
USB	USB High-Speed USB 2.0 OTG/HOST, USB High-Speed USB 2.0
OTHER I/O	3xUART / 2xSDIO / I2C / SPI / EIM / GPIO / 2xSSI / AC97 / I2S

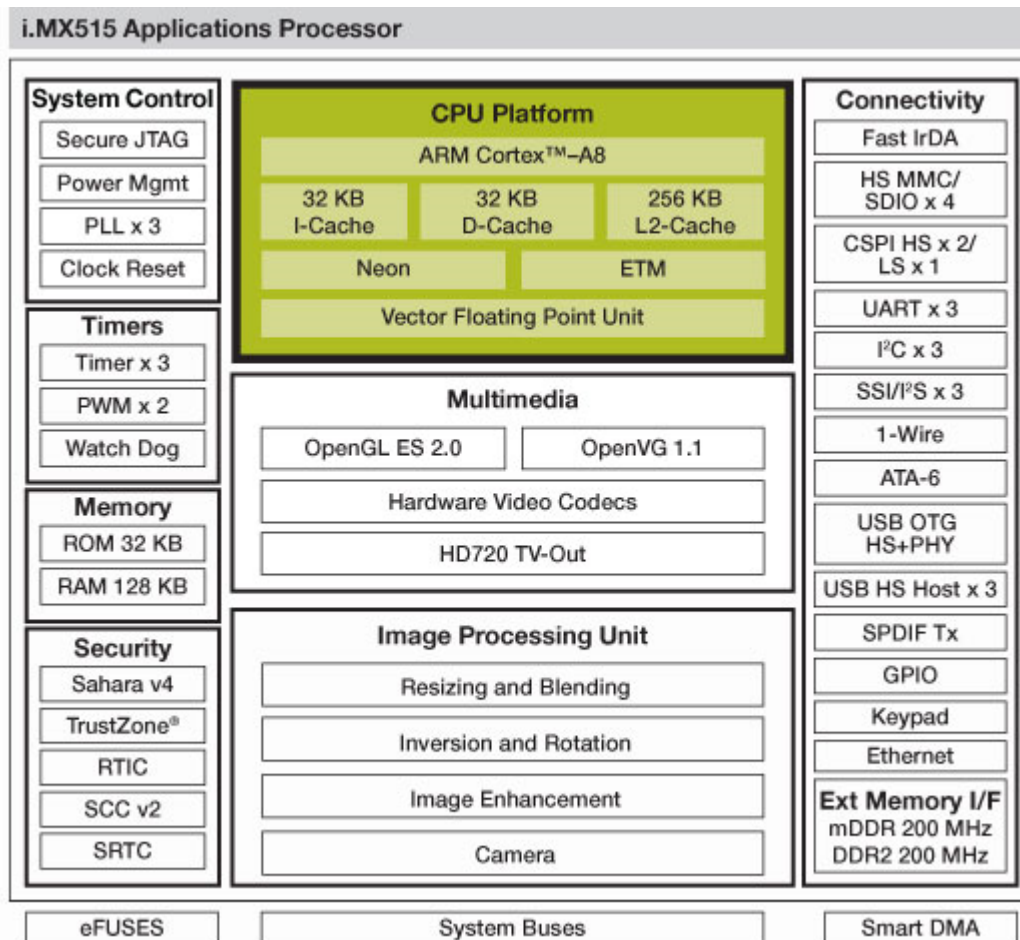
1.4. Reference Documents

For more detailed technical information about the i.MX51 SODIMM module components, please refer to the web resources and documents listed below.

Component	Description
i.MX51 (Freescale) Processor	Freescale_data_sheet_iMX51.pdf
MICRON NAND Flash Memory	MT29F1G08ABBD4HC , MT29F2G08ABBE4HC , MT29F4G08ABBD4HC
MICRON SDRAM Memory	MT47H16M16BG-5E , MT47H32M16HR-3 , MT47H64M16HR-3
SMSC LAN8700 Ethernet Controller	SMSC LAN8700.pdf
Power Management and User Interface IC	freescale.com/data sheet MC13892.pdf
I2C EEPROM	Atmel AT24C512BN-SH-B.pdf

2. Functional Processor Description

2.1. Block Diagram



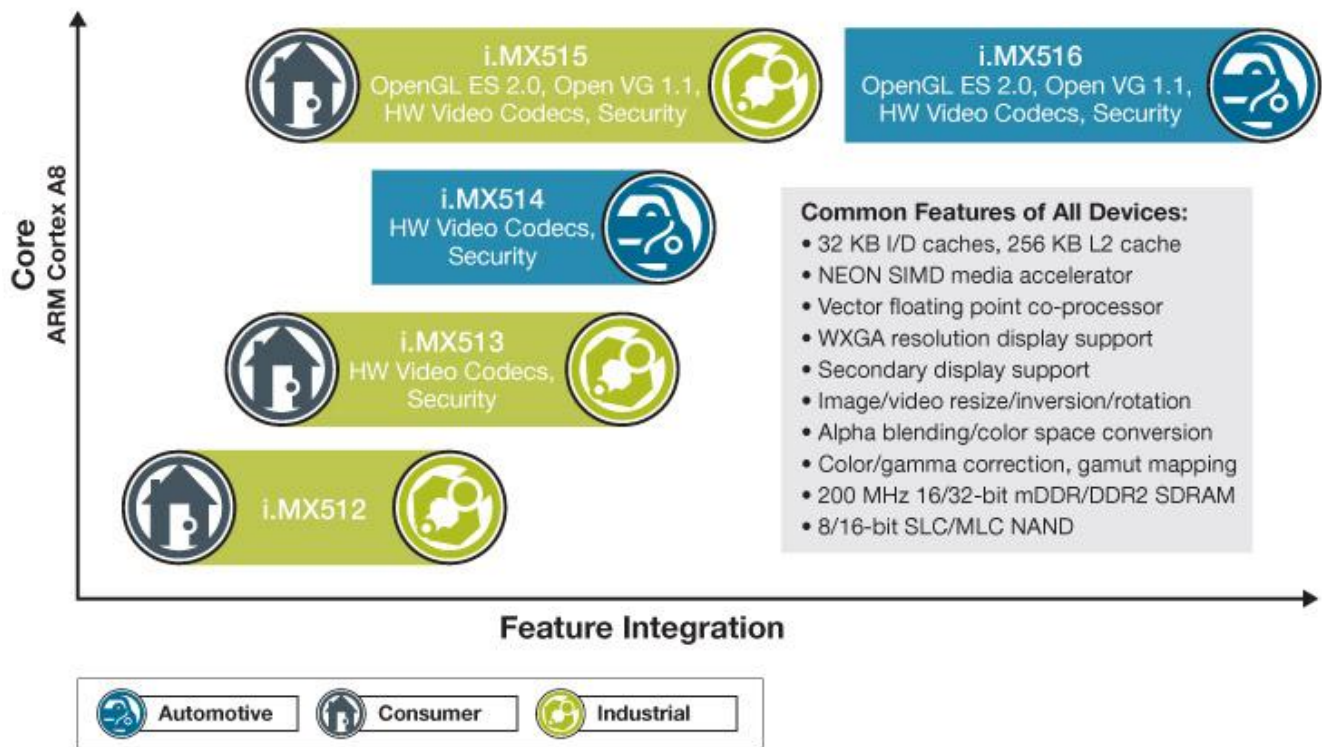
More information in interactive table on [Freescale's webpage](#)

The i.MX515 processor features Freescale's advanced and power-efficient implementation of the ARM Cortex A8™ core, which operates at speeds as high as 800 MHz. Up to 200 MHz DDR2 and mobile DDR DRAM clock rates are supported. The CPU is suitable for the following applications:

- | | |
|---|--|
| • Netbooks (web tablets) | • Portable navigation devices (PND) |
| • Nettops (internet desktop devices) | • High-end PDAs |
| • Mobile internet devices (MID) | • Gaming consoles |
| • Portable media players (PMP) | • Automotive navigation and entertainment (see automotive data sheet, IMX51AEC) |

More information in interactive table on [Freescale's webpage](#)

2.2. Features



i.MX512	
Up to 800MHz (Consumer), 600 MHz (Industrial)	
Target Applications:	- Factory Automation - HMI - Portable/Tethered Printers - Medical Devices - Ebooks

i.MX513	
Up to 800MHz (Consumer), 600 MHz (Industrial)	
Target Applications:	- IP Camera - V2IP Media Phones - Digital Signage - HMI - Medical Devices

i.MX514	
Up to 600 MHz	
Target Applications:	- Navigation - Advanced HMI - Instrument Cluster - Telematics

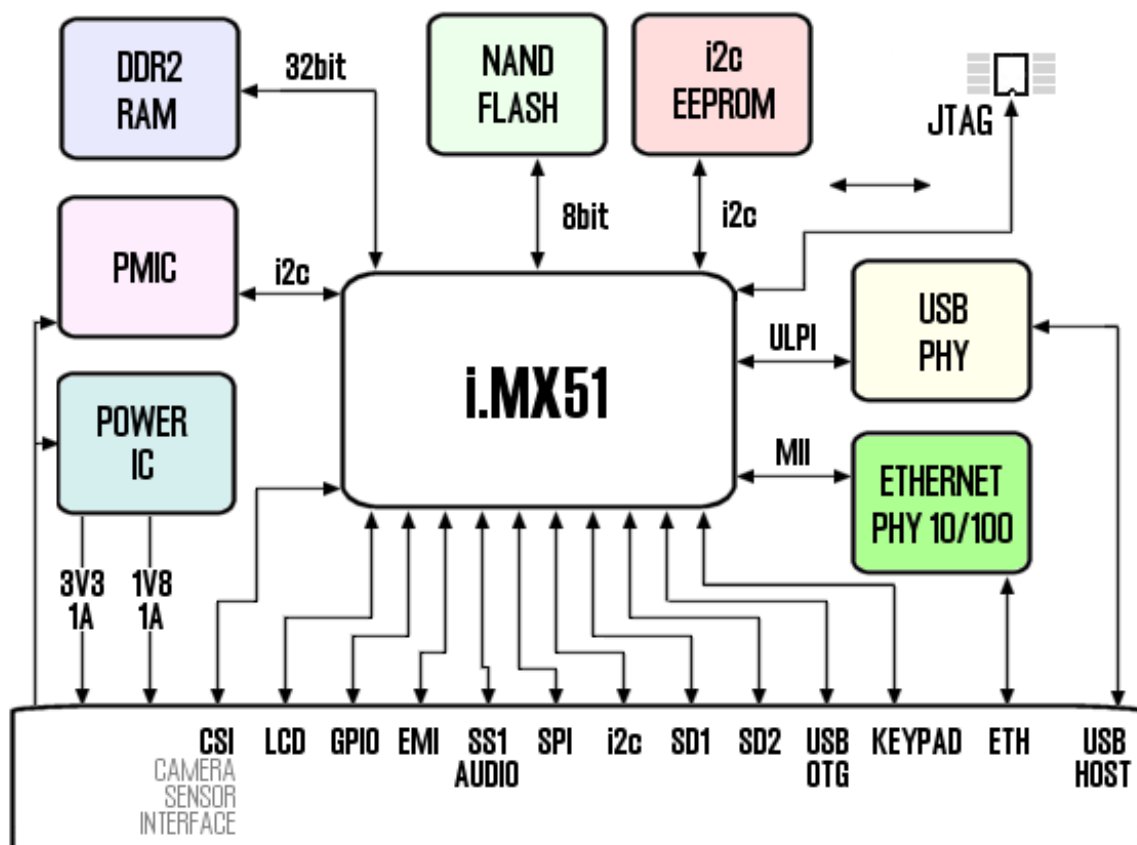
i.MX515	
Up to 800MHz (Consumer), 600 MHz (Industrial)	
Target Applications:	- Smartbook - Mobile Internet Devices - PMPs - Secure Devices - Advanced HMI - High-End PDAs

i.MX516	
Up to 600MHz	
Target Applications:	- Infotainment - Rear Seat Entertainment

3. SODIMM Signal Description

This chapter describes the signals of the Voipac i.MX51 SODIMM module. Some pins have dedicated functionality, but most are highly multiplexed, so that the same pin can have up to 6 different roles and the same functionality is sometimes available alternatively on different pins. Each of these multiplexed pins is additionally also usable as a General Purpose Input/Output pin (GPIO). Additionally each GPIO pin can be used as interrupt source.

3.1. SODIMM Module Block Diagram



3.2. IO Types Notation

Signal	Description
1V8 or 3V3	Digital Signal Voltage Level
ANG	Analog Signal
GND	Ground
PWR	Power supply

3.3. Pin-out Description

Pin	Baseboard	Module	Functions	Type	Description
1	VIN			PWR	Module power supply input (3.0V-5.5V)
2	VIN			PWR	
3	VIN			PWR	
4	VIN			PWR	
5	VIO	PWR_SW2		PWR	1.8V power supply output (up to 1A)
6	VIO	PWR_SW2		PWR	
7	VIO	PWR_SW2		PWR	
8	BOOT MODE	IMX_BOOT_MODE	src_BOOT_MODE[0] src_BOOT_MODE[1]	1V8	Boot mode select H: Serial Downloader / L: Internal Boot
9	VOUT	PWR_SW1		PWR	3.3V power supply output (up to 1A)
10	VOUT	PWR_SW1		PWR	
11	VOUT	PWR_SW1		PWR	
12	VOUT	PWR_SW1		PWR	
13	VBACKUP	PMIC_LICELL		2V5 to 3V3	Provides a connection for a coin cell backup battery or supercap. If the main battery is deeply discharged, removed, or contact-bounced, the RTC system and coin cell maintained logic will switch over to the LICELL for backup power. This pin can be connected to a rechargeable cell or a supercap when used with trickle charge feature.
14	POWER_ON	PMIC_PWRON1		UP to VIN	Power on/off button connection. A turn on event can be accomplished by connecting an open drain NMOS driver.
15	RESET_OUT	IMX_DI1_PIN13	gpio3_GPIO[2]	1V8	This pin is connected to the GPIO to serve as reset.
16	POR_IN	IMX_POR_B	src_POR_B	UP to VIN	Power on reset
17	RESET_IN	IMX_RESET_IN_B PMIC_RESETB	src_RESET_B	1V8	Master Reset – External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module, SDRAMC module, and the clock control module) are reset.

Pin	Baseboard	Module	Functions	Type	Description
18	GND	GND		GND	
ETHERNET					
19	PHY_TXN	LAN_TXN		ANG	Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	PHY_LINK	LAN_LINK		3V3	Active low LINK ON indication: Active indicates that the link is on.
21	PHY_TXP	LAN_TXP		ANG	Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	PHY_VDD	LAN_VDD33		PWR	+3.3V analog power supply output to magnetics
23	PHY_RXN	LAN_RXP		ANG	Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	PHY_ACT	LAN_ACTIVITY		3V3	Active low ACTIVITY indication: Active indicates that there is Carrier sense (CRS) from the active PMD.
25	PHY_RXP	LAN_RXN		ANG	Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND		GND	
USB HOST					
27	USB_VBUS_EN	USB_CPEN		3V3	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
28	USBH_OC	IMX_GPIO1_6	gpio1_GPIO[6]	1V8	Active low over-current indicator input connected to a GPIO.
			ccm_SSI_EXT2_CLK		
			epit2_EPITO		
			gpt_CAPIN2		
29	USBH_DM	USB_DM		ANG	D- pin of the USB cable
30	USBH_VBUS	USB_VBUS		5V	
31	USBH_DP	USB_DP		ANG	D+ pin of the USB cable
32	GND	GND		GND	
USB OTG					
33	USBO_ID	IMX_ID		ANG	ID pin of the USB cable. For an A-Device ID is grounded. For a Bdevice ID is floated.
34	USBO_VBUS_EN	IMX_GPIO1_8	gpio1_GPIO[8]	1V8	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
			usboh3_USB_PWR		
			ccm_CLKO2		
			esdhc2_CD		
35	USBO_DM	IMX_DN		ANG	D- pin of the USB cable
36	USBO_OC	IMX_GPIO1_9	gpio1_GPIO[9]	1V8	Active low over-current indicator input connected to a GPIO. 10KΩ pull-up resistor.
			usboh3_USB_OC		
			ccm_CLKO		

Pin	Baseboard	Module	Functions	Type	Description
			esdhc2_LCTL		
37	USBO_DP	IMX_DP		ANG	D+ pin of the USB cable
38	USBO_VBUS	IMX_VBUS		5V	VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
39	GND	GND		GND	
I2C INTERFACE					
40	I2C DATA	IMX_EIM_D16	gpio2_GPIO[0]	1V8	I2C Data
			uart2_CTS		
			i2c1_SDA		
			audmux_AUD4_RXFS		
			audmux_AUD5_TXD		
41	I2C CLK	IMX_EIM_D19	gpio1_GPIO[2]	1V8	I2C Clock
			uart2_RTS		
			i2c1_SCL		
			audmux_AUD4_RXC		
			audmux_AUD5_TXFS		
PWM INTERFACE					
42	PWM	IMX_GPIO1_2	gpio1_GPIO[2]	1V8	PWM Output
			pwm1_PWMO		
			i2c2_SCL		
1 WIRE INTERFACE					
43	O WIRE	IMX_OWIRE_LINE	owire_LINE	1V8	
			gpio1_GPIO[24]		
			spdif_OUT1		
			src_SYSTEM_RST		
SPI INTERFACE					
44	CSPI_SS0	IMX_CSPI1_SS0	ecspi1_SS0	1V8	Slave Select (Selectable polarity) signal
			audmux_AUD4_TXC		
			gpio4_GPIO[24]		
45	CSPI_SS1	IMX_CSPI1_SS1	ecspi1_SS1	1V8	Slave Select (Selectable polarity) signal
			audmux_AUD4_TXD		
			gpio4_GPIO[25]		
46	CSPI_MOSI	IMX_CSPI1_MOSI	ecspi1_MOSI	1V8	Master Out/Slave In signal
			i2c1_SDA		
			gpio4_GPIO[22]		
47	CSPI_MISO	IMX_CSPI1_MISO	ecspi1_MISO	1V8	Master In/Slave Out signal
			audmux_AUD4_RXD		
			gpio4_GPIO[23]		
48	CSP_CLK	IMX_CSPI1_SCLK	ecspi1_SCLK	1V8	Serial Clock signal
			i2c1_SCL		
			gpio4_GPIO[27]		

Pin	Baseboard	Module	Functions	Type	Description
49	CSPI_RDY	IMX_CSPI1_RDY	ecspi1_RDY	1V8	Serial Data Ready signal
			audmux_AUD4_TXFS		
			gpio4_GPIO[26]		
50	GND	GND		GND	
SD1 INTERFACE					
51	SD1_CD	IMX_NANDE_D12	gpio3_GPIO[28]	1V8	SD Card Detect
52	SD1_D0	IMX_SD1_DATA0	esdhc1_DAT0	1V8	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
			audmux_AUD5_TXD		
			cspi_MISO		
53	SD1_D1	IMX_SD1_DATA1	esdhc1_DAT1	1V8	
			audmux_AUD5_RXD		
54	SD1_D2	IMX_SD1_DATA2	esdhc1_DAT2	1V8	
			audmux_AUD5_TXC		
55	SD1_D3	IMX_SD1_DATA3	esdhc1_DAT3	1V8	
			audmux_AUD5_TXFS		
			cspi_SS1		
56	SD1_CMD	IMX_SD1_CMD	esdhc1_CMD	1V8	SD Command (bidirectional signal)
			audmux_AUD5_RXFS		
			cspi_MOSI		
57	SD1_CLK	IMX_SD1_CLK	esdhc1_CLK	1V8	SD Output Clock.
			audmux_AUD5_RXC		
			cspi_SCLK		
58	GND	GND		GND	
UART1 INTERFACE					
59	UART1_TXD	IMX_UART1_TXD	uart1_TXD_MUX	1V8	Transmit Data output signal
			pwm2_PWMO		
			gpio4_GPIO[29]		
60	UART1_RXD	IMX_UART1_RXD	uart1_RXD_MUX	1V8	Receive Data input signal
			gpio4_GPIO[28]		
61	UART1_RTS	IMX_UART1_RTS	uart1_RTS	1V8	Request to Send input signal
			gpio4_GPIO[30]		
62	UART1_CTS	IMX_UART1_CTS	uart1_CTS	1V8	Clear to Send output signal
			gpio4_GPIO[31]		
UART2 INTERFACE					
63	UART2_TXD	IMX_UART2_TXD	uart2_TXD_MUX	1V8	Transmit Data output signal
			firi_RXD		
			gpio1_GPIO[21]		
64	UART2_RXD	IMX_UART2_RXD	uart2_RXD_MUX	1V8	Receive Data input signal
			firi_TXD		
			gpio1_GPIO[20]		

Pin	Baseboard	Module	Functions	Type	Description
65	UART2_RTS	IMX_EIM_D26	kpp_COL[7]	1V8	Request to Send input signal
			uart3_TXD_MUX		
			uart2_RTS		
			gpt_CMPOUT2		
66	UART2_CTS	IMX_EIM_D25	uart1_DSR	1V8	Clear to Send output signal
			uart3_RXD_MUX		
			uart2_CTS		
			gpt_CMPOUT1		
UART3 INTERFACE					
67	UART3_TXD	IMX_UART3_TXD	uart1_DSR	1V8	Transmit Data output signal
			uart3_TXD_MUX		
			gpio1_GPIO[23]		
68	UART3_RXD	IMX_UART3_RXD	uart1_DTR	1V8	Receive Data input signal
			uart3_RXD_MUX		
			gpio1_GPIO[22]		
69	UART3_RTS	IMX_EIM_D18	gpio2_GPIO[2]	1V8	Request to Send input signal
			uart2_TXD_MUX		
			uart3_RTS		
			audmux_AUD5_TXC		
70	UART3_CTS	IMX_EIM_D17	gpio2_GPIO[1]	1V8	Clear to Send output signal
			uart2_RXD+MUX		
			uart3_CTS		
			audmux_AUD5_RXD		
71	GND	GND		GND	
KEYPAD INTERFACE					
72	KP_COL0	IMX_KEY_COL0	kpp_COL[0]	1V8	Keypad Column selection signals.
73	KP_COL1	IMX_KEY_COL1	kpp_COL[1]	1V8	
74	KP_COL2	IMX_KEY_COL2	kpp_COL[2]	1V8	
75	KP_COL3	IMX_KEY_COL3	kpp_COL[3]	1V8	
			src_INT_BOOT		
76	KP_COL4	IMX_KEY_COL4	kpp_COL[4]	1V8	
			uart1_RI		
			uart3_RTS		
			i2c2_SCL		
			spdif_OUT1		
77	KP_ROW0	IMX_KEY_ROW0	kpp_ROW[0]	1V8	Keypad Row selection signals.
78	KP_ROW1	IMX_KEY_ROW1	kpp_ROW[1]	1V8	
79	KP_ROW2	IMX_KEY_ROW2	kpp_ROW[2]	1V8	
80	KP_ROW3	IMX_KEY_ROW3	kpp_ROW[3]	1V8	
81	KP_COL5	IMX_KEY_COL5	kpp_COL[5]	1V8	Keypad column selection signal

Pin	Baseboard	Module	Functions	Type	Description
			uart1_DCD		
			uart3_CTS		
			i2c2_SDA		
82	GND	GND		GND	
SSI1 INTERFACE					
83	SSI1_INT	IMX_DI1_D0_CS	gpio3_GPIO[3]	1V8	SSI Interrupt
84	SSI1_RXD	IMX_AUD3_BB_RXD	audmux_AUD3_RXD	1V8	Receive serial data
			uart3_RXD_MUX		
			gpio4_GPIO[19]		
85	SSI1_TXD	IMX_AUD3_BB_TXD	audmux_AUD3_TXD	1V8	Transmit serial data
			gpio4_GPIO[18]		
86	SSI1_CLK	IMX_AUD3_BB_CK	audmux_AUD3_TXC	1V8	Serial clock
			gpio4_GPIO[20]		
87	SSI1_FS	IMX_AUD3_BB_FS	audmux_AUD3_TXFS	1V8	Frame Sync
			uart3_TXD_MUX		
			gpio4_GPIO[21]		
88	GND	GND		GND	
SSI2 INTERFACE					
89	SSI2_INT	IMX_DI1_D1_CS	gpio3_GPIO[4]	1V8	SSI Interrupt
90	SSI2_RXD	IMX_EIM_D29	kpp_ROW[5]	1V8	Receive serial data
			audmux_AUD6_RXD		
91	SSI2_TXD	IMX_EIM_D28	kpp_ROW[4]	1V8	Transmit serial data
			audmux_AUD6_TXD		
92	SSI2_CLK	IMX_EIM_D30	kpp_ROW[6]	1V8	Serial clock
			audmux_AUD6_TXC		
93	SSI2_FS	IMX_EIM_D31	kpp_ROW[7]	1V8	Frame Sync
			audmux_AUD6_TXFS		
94	GND	GND		GND	
SD2 INTERFACE					
95	SD2_CD	IMX_NANDF_D13	gpio3_GPIO[27]	1V8	SD Card Detect
96	SD2_D0	IMX_SD2_DATA0	esdhc2_DAT0	1V8	SD Data (bidirectional signal) - If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added
			esdhc1_DAT4		
			cspi_MISO		
97	SD2_D1	IMX_SD2_DATA1	esdhc2_DAT1	1V8	
			esdhc1_DAT5		
			usboh3_H2_DP		
98	SD2_D2	IMX_SD2_DATA2	esdhc2_DAT2	1V8	
			esdhc1_DAT6		
			usboh3_H2_DM		
99	SD2_D3	IMX_SD2_DATA3	esdhc2_DAT3	1V8	

Pin	Baseboard	Module	Functions	Type	Description
100	SD2_CMD	IMX_SD2_CMD	esdhc1_DAT7	1V8	SD command bidirectional signal
			cspi_SS2		
			esdhc2_CMD		
			i2c1_SCL		
101	SD2_CLK	IMX_SD2_CLK	cspi_MOSI	1V8	SD Output Clock
			esdhc2_CLK		
			i2c1_SDA		
102	GND	GND	cspi_SCLK	GND	
CMOS SENSOR INTERFACE					
103	CSI_D0	IMX_CSI2_D12	CSI2_D[12]	1V8	Sensor port data
			gpio4_GPIO[9]		
104	CSI_D1	IMX_CSI2_D13	CSI2_D[13]	1V8	Sensor port data
			gpio4_GPIO[10]		
105	CSI_D2	IMX_CSI2_D14	CSI2_D[14]	1V8	Sensor port data
106	CSI_D3	IMX_CSI2_D15	CSI2_D[15]	1V8	Sensor port data
107	CSI_D4	IMX_CSI2_D16	CSI2_D[16]	1V8	Sensor port data
108	CSI_D5	IMX_CSI2_D17	CSI2_D[17]	1V8	Sensor port data
109	CSI_D6	IMX_CSI2_D18	CSI2_D[18]	1V8	Sensor port data
			gpio4_GPIO[11]		
110	CSI_D7	IMX_CSI2_D19	CSI2_D[19]	1V8	Sensor port data
			gpio4_GPIO[12]		
111	GND	GND		GND	
112	CSI_HSYNC	IMX_CSI2_HSYNC	CSI2_VSYNC	1V8	Horizontal Sync (Start Of Frame)
			gpio4_GPIO[13]		
113	CSI_VSYNC	IMX_CSI2_VSYNC	CSI2_HSYNC	1V8	Vertical Sync (Blank Signal)
			gpio4_GPIO[14]		
114	CSI_PCLK	IMX_CSI2_PIXCLK	CSI2_PIXCLK	1V8	Sensor data latch clock (Pixel Clock)
			gpio4_GPIO[15]		
115	CSI_MCLK	CSI_MCLK	gpio1_GPIO[5]	1V8	Sensor Master Clock
			wdog2_WDOG_B		
			ccm_CLKO		
			ccm_CSI2_MCLK		
116	GND			GND	
LCD INTERFACE					
117	LCD_D0	IMX_DISP1_DAT0	ipu_DISP1_DAT[0]	1V8	LCD Data Bus
118	LCD_D1	IMX_DISP1_DAT1	ipu_DISP1_DAT[1]	1V8	LCD Data Bus
119	LCD_D2	IMX_DISP1_DAT2	ipu_DISP1_DAT[2]	1V8	LCD Data Bus
120	LCD_D3	IMX_DISP1_DAT3	ipu_DISP1_DAT[3]	1V8	LCD Data Bus
121	LCD_D4	IMX_DISP1_DAT4	ipu_DISP1_DAT[4]	1V8	LCD Data Bus

Pin	Baseboard	Module	Functions	Type	Description
122	LCD_D5	IMX_DISP1_DAT5	ipu_DISP1_DAT[5]	1V8	LCD Data Bus
123	LCD_D6	IMX_DISP1_DAT6	ipu_DISP1_DAT[6] src_BT_USB_SRC	1V8	LCD Data Bus
124	LCD_D7	IMX_DISP1_DAT7	ipu_DISP1_DAT[7] src_BT_EEPROM_CFG	1V8	LCD Data Bus
125	LCD_D8	IMX_DISP1_DAT8	ipu_DISP1_DAT[8] src_BT_SRC[0]	1V8	LCD Data Bus
126	LCD_D9	IMX_DISP1_DAT9	ipu_DISP1_DAT[9] src_BT_SRC[1]	1V8	LCD Data Bus
127	LCD_D10	IMX_DISP1_DAT10	ipu_DISP1_DAT[10] src_BT_SPARE_SIZE	1V8	LCD Data Bus
128	LCD_D11	IMX_DISP1_DAT11	ipu_DISP1_DAT[11] src_BT_LPB_FREQ[2]	1V8	LCD Data Bus
129	GND	GND		GND	
130	LCD_D12	IMX_DISP1_DAT12	ipu_DISP1_DAT[12] src_MLC_SEL	1V8	LCD Data Bus
131	LCD_D13	IMX_DISP1_DAT13	ipu_DISP1_DAT[13] src_BT_MEM_CTL[0]	1V8	LCD Data Bus
132	LCD_D14	IMX_DISP1_DAT14	ipu_DISP1_DAT[14] src_BT_MEM_CTL[1]	1V8	LCD Data Bus
133	LCD_D15	IMX_DISP1_DAT15	ipu_DISP1_DAT[15] src_BT_BUS_WIDTH	1V8	LCD Data Bus
134	LCD_D16	IMX_DISP1_DAT16	ipu_DISP1_DAT[16] src_BT_PAGE_SIZE[0]	1V8	LCD Data Bus
135	LCD_D17	IMX_DISP1_DAT17	ipu_DISP1_DAT[17] src_BT_PAGE_SIZE[1]	1V8	LCD Data Bus
136	LCD_D18	IMX_DISP1_DAT18	ipu_DISP1_DAT[18] src_BT_WEIM_MUXED[0]	1V8	LCD Data Bus
137	LCD_D19	IMX_DISP1_DAT19	ipu_DISP1_DAT[19] src_BT_WEIM_MUXED[1]	1V8	LCD Data Bus
138	LCD_D20	IMX_DISP1_DAT20	ipu_DISP1_DAT[20] src_BT_MEM_TYPE[0]	1V8	LCD Data Bus
139	LCD_D21	IMX_DISP1_DAT21	ipu_DISP1_DAT[21] src_BT_MEM_TYPE[1]	1V8	LCD Data Bus
140	LCD_D22	IMX_DISP1_DAT22	ipu_DISP1_DAT[22] src_BT_LPB_FREQ[0]	1V8	LCD Data Bus
141	LCD_D23	IMX_DISP1_DAT23	src_BT_LPB_FREQ[0] src_BT_LPB_FREQ[1]	1V8	LCD Data Bus
142	GND	GND		GND	
143	LCD_HSYNC	IMX_DI1_PIN2	ipu_DI1_PIN2	1V8	Line Pulse or HSync

Pin	Baseboard	Module	Functions	Type	Description
144	LCD_VSYNC	IMX_DI1_PIN3	ipu_DI1_PIN3	1V8	Frame Sync or Vsync
145	LCD_OE_ACD	IMX_DI1_PIN15	ipu_DI1_PIN15	1V8	Alternate Crystal Direction/Output Enable
146	LCD_LSCLK	IMX_DI1_DISP_CLK	ipu_DI1_DISP_CLK	1V8	Shift Clock
147	GND	GND		GND	
GPIO INTERFACE/ MODULE SPECIFIC SIGNALS					
148	GPIO0	IMX_GPIO1_0	esdhc1_CD gpio1_GPIO[0] cspi_SS1	1V8	GPIO1_0
149	GPIO1	IMX_GPIO1_1	esdhc1_WP gpio1_GPIO[1] cspi_MISO	1V8	GPIO1_1
150	GPIO2	IMX_EIM_D20	gpio2_GPIO[4] audmux_AUD4_TXD	1V8	GPIO2_4
151	GPIO3	IMX_EIM_D21	gpio2_GPIO[5] audmux_AUD4_RXD	1V8	GPIO2_5
152	GPIO4	IMX_EIM_D22	gpio2_GPIO[6] audmux_AUD4_TXC	1V8	GPIO2_6
153	GPIO5	IMX_EIM_D23	gpio2_GPIO[7] spdif_OUT1 audmux_AUD4_TXFS	1V8	GPIO2_7
154	GPIO6	IMX_DI1_PIN11	gpio3_GPIO[0] ecspi1_SS2	1V8	GPIO3_0
155	GPIO7	IMX_DI1_PIN12	gpio3_GPIO[1]	1V8	GPIO3_1
156	GPIO8	IMX_DISP2_SER_DIN	gpio3_GPIO[5]	1V8	GPIO3_5
157	GPIO9	IMX_DISP2_SER_DIO	gpio3_GPIO[6] wdog1_WDOG_RST_B_DEB	1V8	GPIO3_6
158	GPIO10	IMX_DISP2_SER_CLK	gpio3_GPIO[7] wdog2_WDOG_RST_B_DEB	1V8	GPIO3_7
159	GPIO11	IMX_DISP2_SER_RS	gpio3_GPIO[8]	1V8	GPIO3_8
160	GND	GND		GND	
EXTERNAL MEMORY INTERFACE					
161	EMI-CS0	MIX_EIM_CS0	emi_EIM_CS0 gio2_GPIO[25]	1V8	
162	EMI-CS1	MIX_EIM_CS1	emi_EIM_CS1 gpio2_GPIO[26]	1V8	
163	EMI-CS4	MIX_EIM_DTACK	emi_WEIM_DTACK_B gpio2_GPIO[31]	1V8	
		EIM_A27	emi_EIM_A[27] gpio2_GPIO[21]		
164	EMI_WAIT	MIX_EIM_WAIT	emi_EIM_WAIT	1V8	

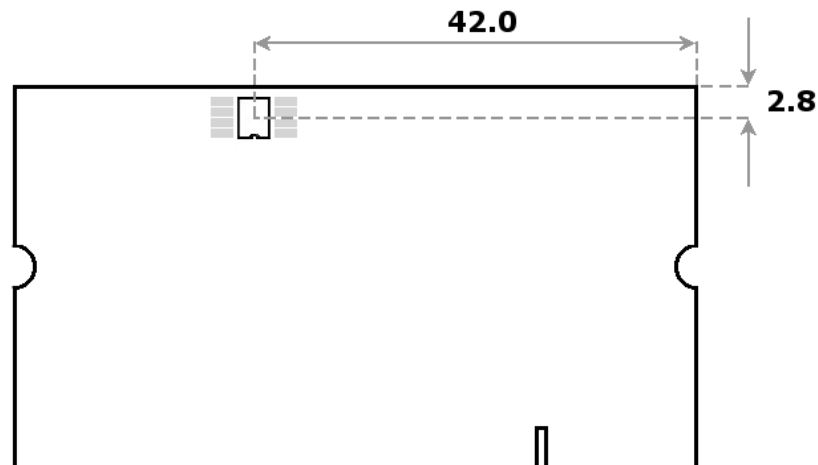
Pin	Baseboard	Module	Functions	Type	Description
165	EMI_EB0	MIX_EIM_EB0	emi_EIM_EB[0]	1V8	
166	EMI_EB1	MIX_EIM_EB1	emi_EIM_EB[1]	1V8	
167	EMI_OE	MIX_EIM_OE	emi_EIM_OE gpio2_GPIO[24]	1V8	
168	EMI_LBA	MIX_EIM_LBA	emi_EIM_LBA gpio3_GPIO[1]	1V8	
169	EMI_RW	MIX_EIM_RW	emi_EIM_RW	1V8	
170	EMI_BCLK	MIX_EIM_BCLK	emi_EIM_BCLK	1V8	
171	GND	GND		GND	
172	EMI_A0	MIX_EIM_A16	emi_EIM_A[16] gpio2_GPIO[10] src_OSC_FREQ_SEL[0]	1V8	
173	EMI_A1	MIX_EIM_A17	emi_EIM_A[17] gpio2_GPIO[11] src_OSC_FREQ_SEL[1]	1V8	
174	EMI_A2	MIX_EIM_A18	emi_EIM_A[18] gpio2_GPIO[12] src_BT_LPB[0]	1V8	
175	EMI_A3	MIX_EIM_A19	emi_EIM_A[19] gpio2_GPIO[13] src_BT_LPB[1]	1V8	
176	EMI_A4	MIX_EIM_A20	emi_EIM_A[20] gpio2_GPIO[14] src_BT_UART_SRC[0]	1V8	
177	EMI_A5	MIX_EIM_A21	emi_EIM_A[21] gpio2_GPIO[15] src_BT_UART_SRC[1]	1V8	
178	EMI_A6	MIX_EIM_A22	emi_EIM_A[22] gpio2_GPIO[16]	1V8	
179	EMI_A7	MIX_EIM_A23	emi_EIM_A[23] gpio2_GPIO[17] src_BT_HPN_EN	1V8	
180	EMI_A8	MIX_EIM_A24	emi_EIM_A[24] gpio2_GPIO[18]	1V8	
181	EMI_A9	MIX_EIM_A25	emi_EIM_A[25] gpio2_GPIO[19]	1V8	
182	EMI_A10	MIX_EIM_A26	emi_EIM_A[26] gpio2_GPIO[20]	1V8	
183	GND	GND		GND	
184	EMI_D0	MIX_EIM_DA0	emi_EIM_DA[0]	1V8	

Pin	Baseboard	Module	Functions	Type	Description
185	EMI_D1	MIX_EIM_DA1	emi_EIM_DA[1]	1V8	
186	EMI_D2	MIX_EIM_DA2	emi_EIM_DA[2]	1V8	
187	EMI_D3	MIX_EIM_DA3	emi_EIM_DA[3]	1V8	
188	EMI_D4	MIX_EIM_DA4	emi_EIM_DA[4]	1V8	
189	EMI_D5	MIX_EIM_DA5	emi_EIM_DA[5]	1V8	
190	EMI_D6	MIX_EIM_DA6	emi_EIM_DA[6]	1V8	
191	EMI_D7	MIX_EIM_DA7	emi_EIM_DA[7]	1V8	
192	EMI_D8	MIX_EIM_DA8	emi_EIM_DA[8]	1V8	
193	EMI_D9	MIX_EIM_DA9	emi_EIM_DA[9]	1V8	
194	EMI_D10	MIX_EIM_DA10	emi_EIM_DA[10]	1V8	
195	EMI_D11	MIX_EIM_DA11	emi_EIM_DA[11]	1V8	
196	EMI_D12	MIX_EIM_DA12	emi_EIM_DA[12]	1V8	
197	EMI_D13	MIX_EIM_DA13	emi_EIM_DA[13]	1V8	
198	EMI_D14	MIX_EIM_DA14	emi_EIM_DA[14]	1V8	
199	EMI_D15	MIX_EIM_DA15	emi_EIM_DA[15]	1V8	
200	GND			GND	

4. Voipac i.MX51 SODIMM module Connectors

4.1. Physical Locations

Along with the main 200pin SODIMM connector the Voipac i.MX51 SODIMM module is equipped with pads for board-to-board pitch compression JTAG connector. The position is shown in the figure below.



Dimensions (in millimeters)

4.2. JTAG

Connector: Molex 47041-0001 www.molex.com

Pin#	Pin Name	Type	Description
1	+1V8	PWR	JTAG interface I/O voltage detect
2	GND	PWR	Ground
3	TMS	IN	JTAG mode select
4	nTRST	IN	JTAG reset
5	TCK	IN	JTAG clock
6	TDO	OUT	JTAG Data output
7	TDI	IN	JTAG Data input
8	nSRST	OUT	System reset

5. Technical Specifications

5.1. Electrical - Power Consumption

Table Part 1

Parameter	VIN	VIO	3V3	
	Pin	Pout	Pout	Pmod
State	[mW]	[mW]	[mW]	[mW]
Barebox	2420,63	-1,82	-82,25	2336,56
Linux	2124,83	-1,82	-783,02	1339,99
Linux (backlight off)	1793,22	-1,82	-546,14	1245,26
Memtest	2788,88	-1,82	-546,14	2240,92

Table Part 2

Test Point	TP100	TP100-101		TP103	TP102-103		TP105	TP104-105	
	U	U	I	U	U	I	U	U	I
State	[V]	[mV]	[mA]	[V]	[mV]	[mA]	[V]	[mV]	[mA]
Barebox	4,91	49,3	493	1,82	-0,1	-1	3,29	-2,5	-25
Linux	4,93	43,1	431	1,82	-0,1	-1	3,29	-23,8	-238
Linux (backlight off)	4,94	36,3	363	1,82	-0,1	-1	3,29	-16,6	-166
Memtest	4,91	56,8	568	1,82	-0,1	-1	3,29	-16,6	-166

5.2. Electrical – DC Characteristics

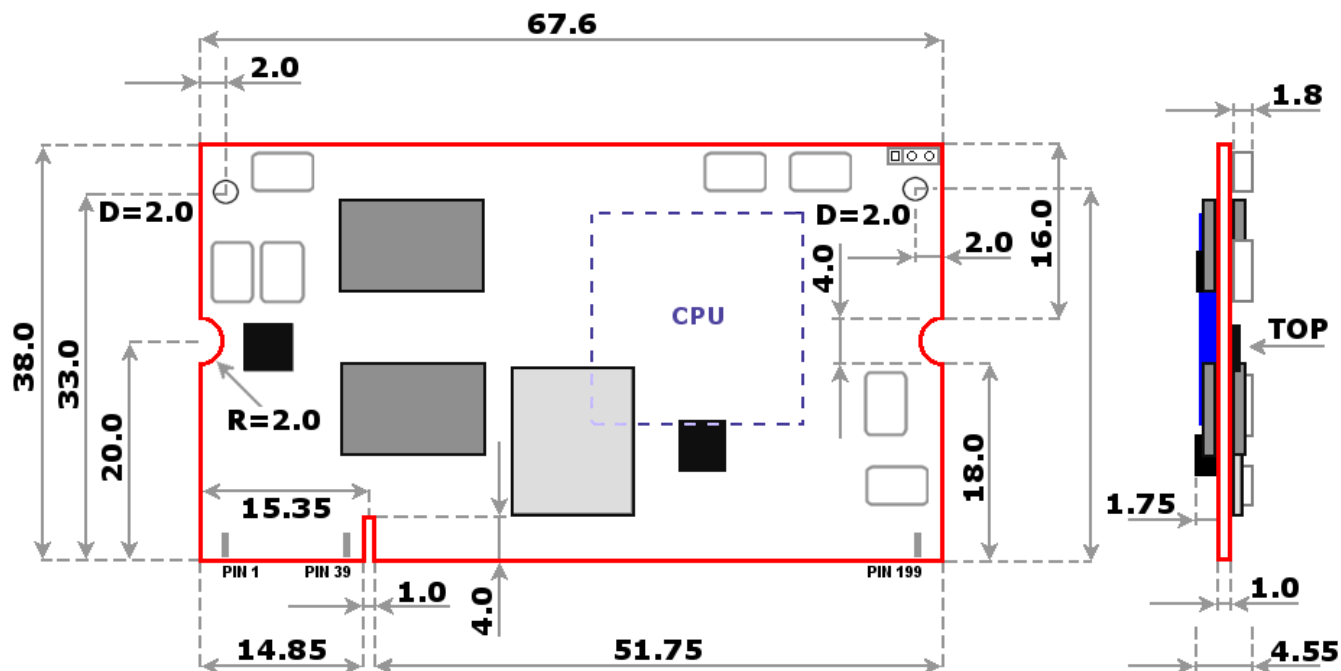
Symbol Description	Min	Typ	Max	Unit
VCC Power supply voltage	4.5	5.0	5.5	V
ARM core supply voltage	1.05	1.1	1.15	V
IDD_800 Operating current at 800MHz (5V)	170	250	500	mA
VIH Digital input high voltage	1.26	-	1.8	V
VIL Digital input low voltage	0	-	0.54	V

5.3. Layer Structure

	PSR	0.015
	Cu Plating	0.03
	Cu	0.012
~~~~~	Prepreg	0.06
	Core	0.1
~~~~~	Prepreg	0.018
	Core	0.06
~~~~~	Prepreg	0.018
	Core	0.1
~~~~~	Prepreg	0.018
	Core	0.06
~~~~~	Prepreg	0.018
	Cu	0.012
	Cu Plating	0.03
	PSR	0.015
	<b>Total</b>	<b>1.018</b>



## Dimensions (in millimeters)



### 5.5. Socket for the Voipac i.MX51 SODIMM module

The Voipac i.MX51 SODIMM module fits into a regular 2.5V DDR1 SODIMM memory socket. More details are available in [Manufacturer's Datasheet](#) or [3D View](#).

### 5.6. Temperature Range

Symbol	Description	Min	Max	Unit	Standard Unit Range
T_AMB	Operating temperature range - COMMERCIAL	0	70	°C	
T_AMB	Operating temperature range - EXTENDED	-20	70	°C	X
T_AMB	Operating temperature range - INDUSTRIAL	-40	85	°C	

## 5.7. RoHS and WEEE Compliance

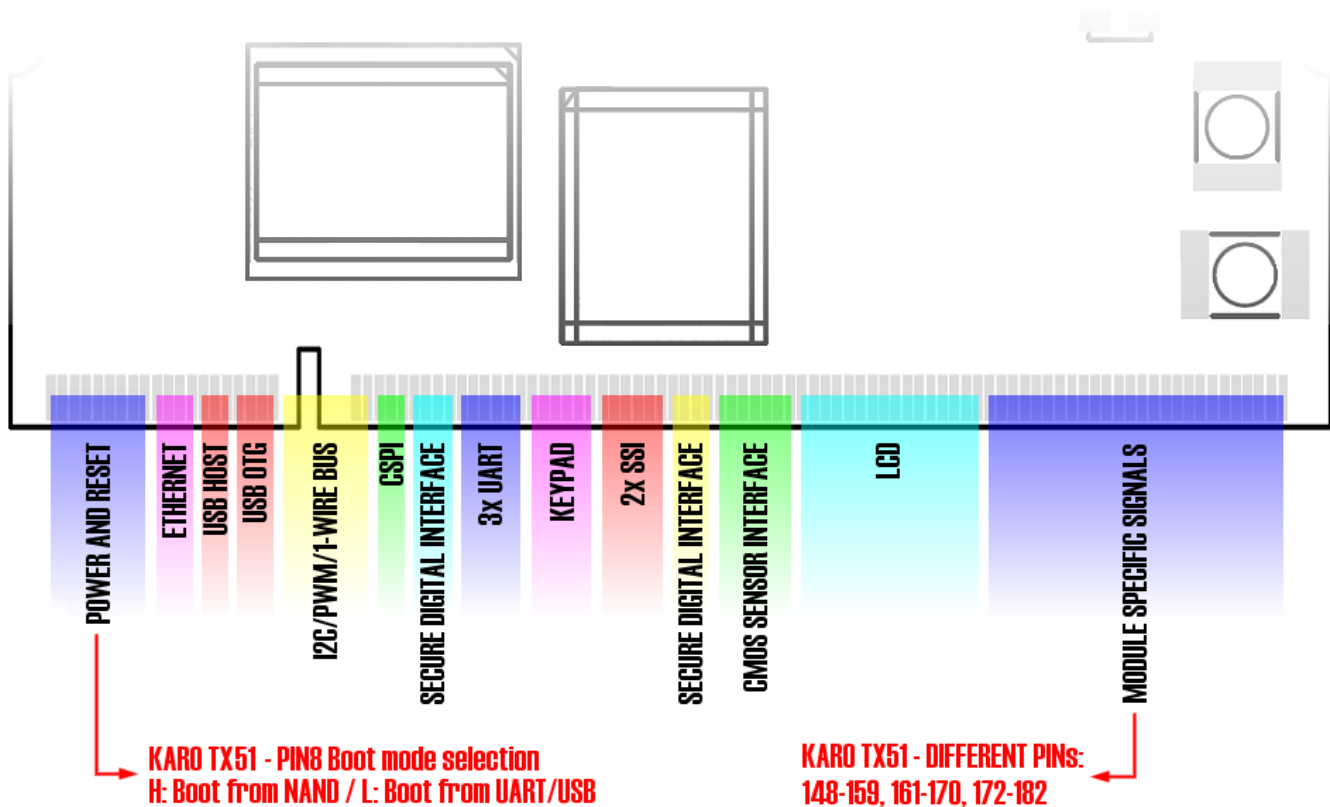
All of the products designed and manufactured by Voipac Technologies are classified as Electrical and Electronic Equipment (EEE) under the Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment 2002/95/EC (RoHS). To comply with the RoHS directive, the restricted use of Lead (Pb), Mercury (Hg), Cadmium (Cd), Hexavalent Chromium (Cr 6+), Polybrominated Biphenyls (PBB) and Polybrominated Diphenyl Ethers (PBDE) must be ensured. Voipac Technologies guarantees that products ordered after July 1, 2006 are assembled in full compliance with the RoHS directive from the European Parliament and Counsel. The company procedures also complies with the Waste Electrical and Electronic Equipment Directive 2002/96/EC (WEEE) .

## 6. Compatibility

Voipac i.MX51 SODIMM module can be used as a replacement for KARO Electronics TX51 Module. This chapter points out the differences for a smooth transition.

### 6.1. KARO Electronics TX51 Module

Voipac i.MX51 SODIMM Module and TX51 from KaRo share the same pin mapping of all SODIMM pins, besides the General Purpose IOs and Module specific signals that may differ. For more details, see the picture below.





## 7. Support

All the relevant communication should be executed via e-mails preferably. Response time is up to 48 hours, except state holidays and weekends. Voipac Technologies working hours are: 8:00 - 17:00, Monday – Friday.

To claim warranty and RMA number assignment, please fill in this [protocol/problem description form](#) and send it to: [reclamations@voipac.com](mailto:reclamations@voipac.com).

Board warranty without the protocol/problem description will not be processed.

For more information, see our [General Terms and Conditions](#).

Besides the free-of-charge support, we provide support for your new designs when it comes to the special drivers for the peripherals not included in the Voipac development kits, design of your own base boards, prototyping, or even new products development, please contact: [support@voipac.com](mailto:support@voipac.com) for more info.

By [registering on Voipac's Internet Customer Details site](#), you will be granted to access the [Voipac Ticketing System](#), where you can post support request tickets and receive e-mail notifications upon any change of your ticket's status.

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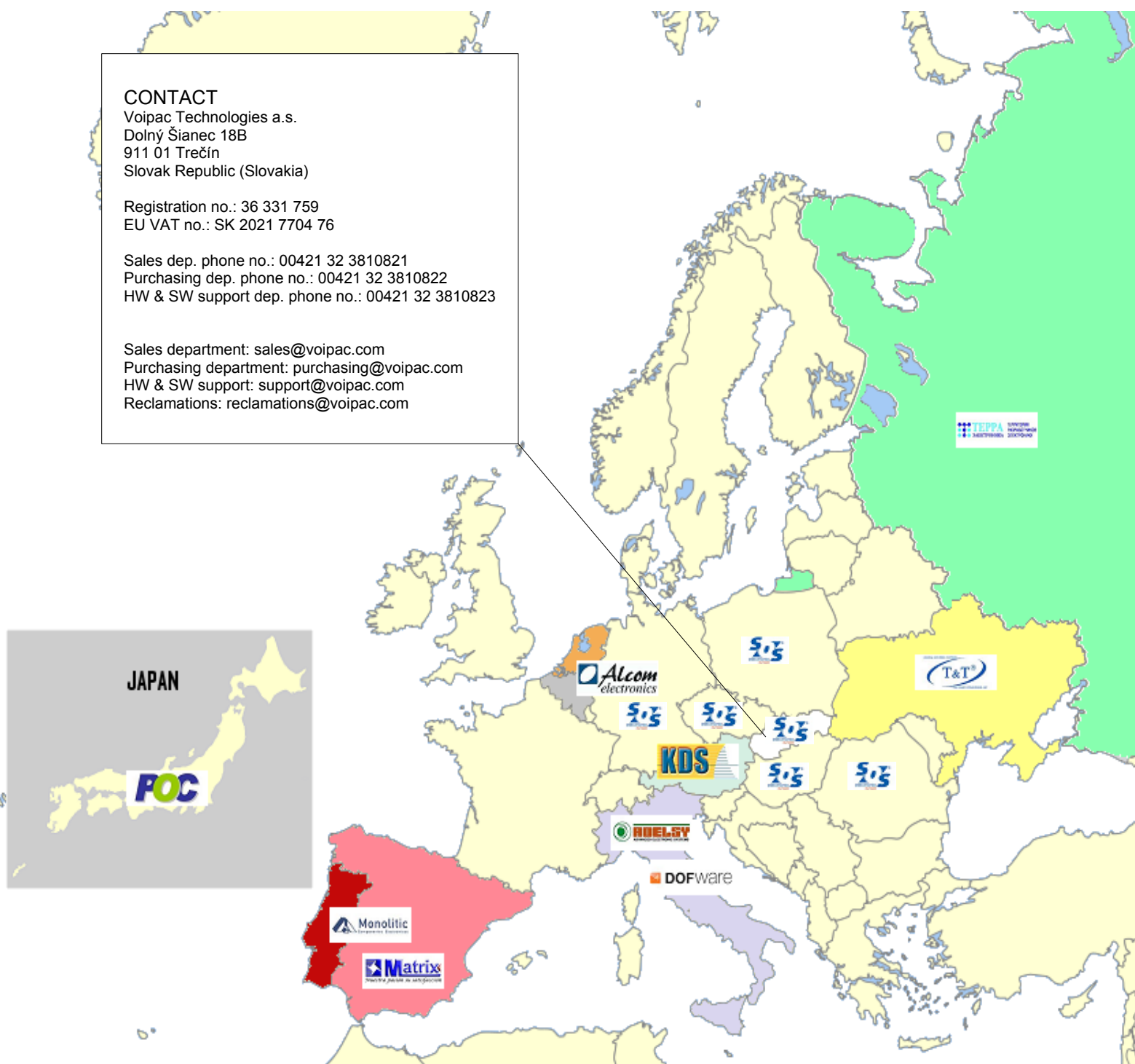
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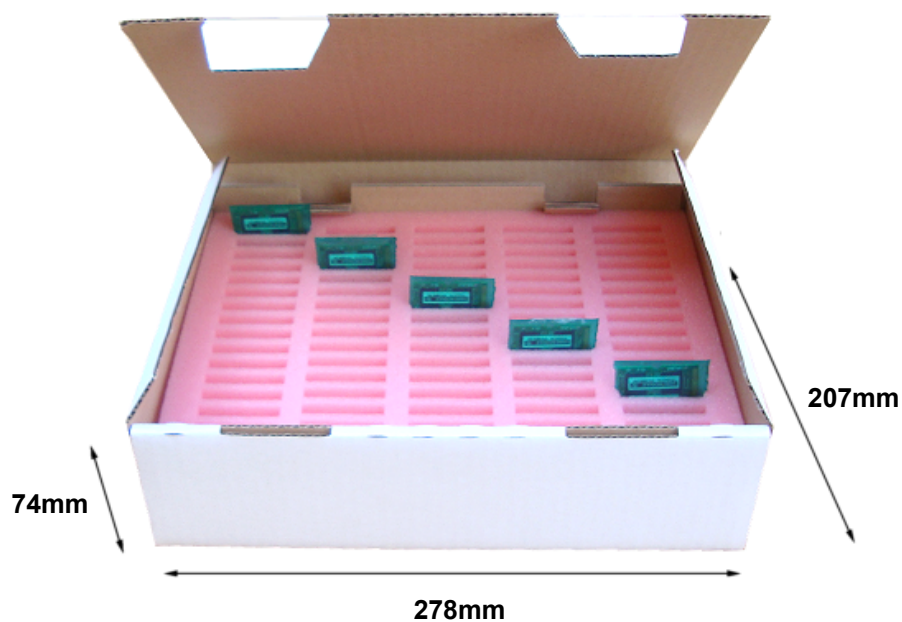
Registration no.: 36 331 759  
EU VAT no.: SK 2021 7704 76

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HW & SW support: support@voipac.com  
Reclamations: reclamations@voipac.com



## 9. Ordering Information



The standard box includes 75pcs of modules, each of them sealed in ESD plastic bag.

## Warranty:

### Voipac Technologies a.s. Does Not Bear Responsibility for the Following:

- Failure of a product resulting from misuse, accident, modification, unsuitable operating environment, or improper maintenance by user
- Unless otherwise agreed in written, a product does not include technical support and the customer may be able to purchase technical support under separate agreement
- Any technical or other support provided under warranty by Voipac Technologies a.s. such as assistance, set-up and installation is provided WITHOUT WARRANTY OF ANY KIND.

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