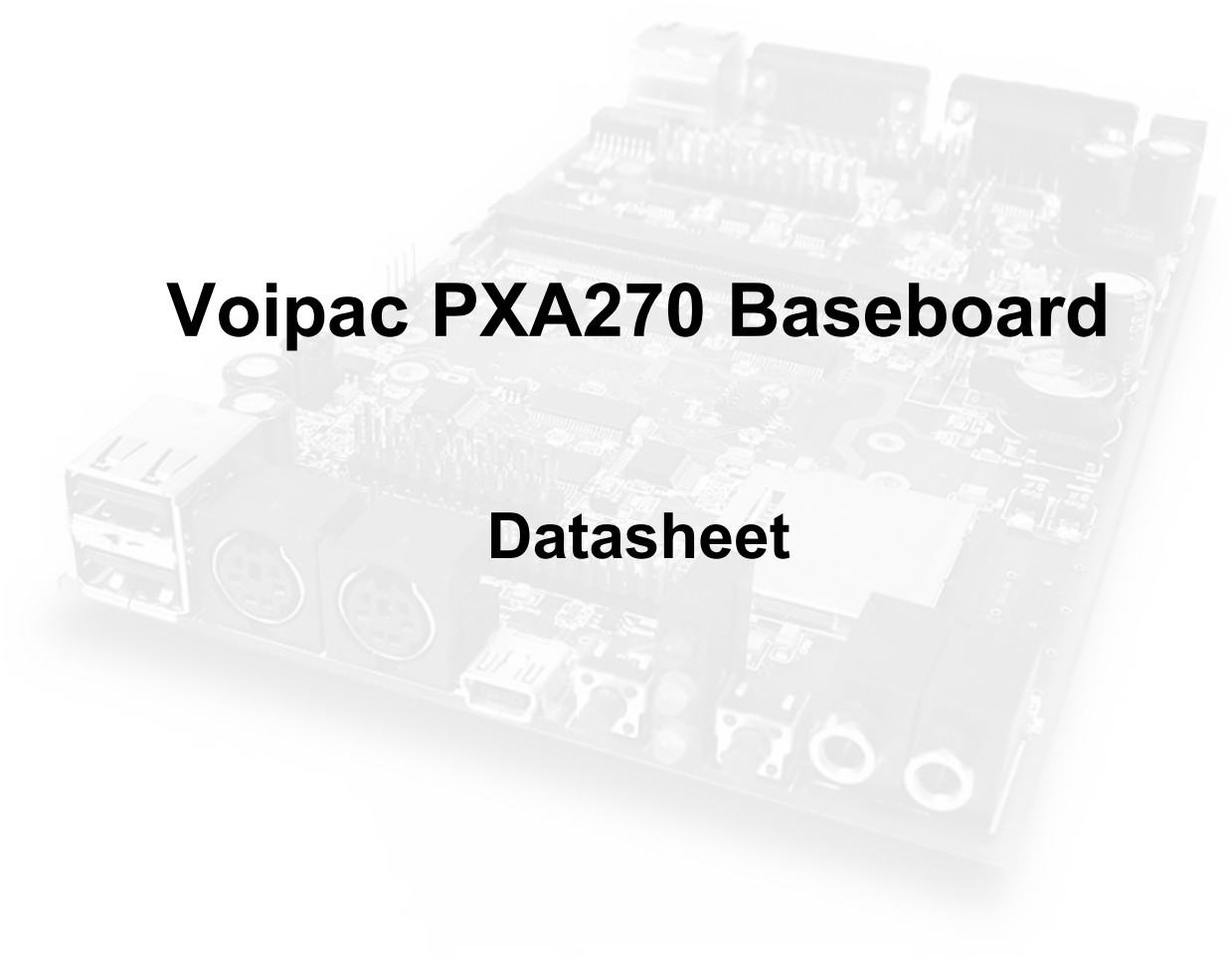


Voipac PXA270 Baseboard

Datasheet

Date	Revision	Changes
28. September 2006	1.0	Initial Release
21. April 2009	1.1	Update
16. March 2011		Added Support and Distributors Chapter

Table of Contents

1. Introduction

1.1 General

Voipac PXA270 baseboard is designed to be used as development platform for Voipac PXA270 module, as well as low power universal industrial PC. Low power system with excellent MIPS/mW performance allows deployment in situation where power source is limited. Besides the standard PC peripheral interfaces it provides numerous communication channels as well as universal expansion slots and connectors.

1.2 Software

Voipac fully supports Linux operating system with drivers for all basic interfaces. Custom additional drivers for specific applications can be developed upon request.

Operating system	Description
Linux	Linux 2.6 with drivers for most common interfaces
Windows CE	Windows CE 6.0 (PXA270 DIMM Module)
QNX	

1.3 Features

Interface	Type	Description
POWER SUPPLY		7-37V, 15W max
SERIAL	DB-9	RS-232, 38400 bps, 8n1
VGA	DB15	1024x768 8/16bit
ETHERNET	RJ-45	10/100 Mbps
IDE	44pin	2,5” IDE HDD, PIO4 / UDMA2 mode, 12 MB/s max
AUDIO OUT	3,5mm JACK	STEREO, R_{load} = 32 Ω
AUDIO IN	3,5mm JACK	LINE IN, MIC
KBD,MOUSE	DIN6	PS/2
USB	USB A / mini USB	1xUSB Host, 1xUSB 2.0 OTG Host/Device

1.4 Reference Documents

For more detailed technical information about the Voipac PXA270 module components, please refer to the web resources and documents listed below.

Component	Description
Intel Xscale® PXA270 Processor	http://voipac.com/fileDownload?fileName=Documents/pxa270dm.pdf
Davicom DM9000E Ethernet Controller	http://www.davicom.com.tw/userfile/24247/DM9000-DS-F03-041906_1.pdf
Philips UCB1400 Audio Controller	http://www.nxp.com/pip/UCB1400BE.html
Maxim MAX1587 Power Controller	http://datasheets.maxim-ic.com/en/ds/MAX1586A-MAX1587C.pdf
Intel StrataFlash® Embedded Memory	http://www.mipsasoft.com/MS7/Hardware/FLASH/StrataFlash P30-T Data Sheet.pdf
SAMSUNG OneNAND™ Flash Memory	http://www.samsung.com/global/business/semiconductor/productList.do?fmly_id=160
SAMSUNG Mobile SDRAM	http://www.samsung.com/global/business/semiconductor/productList.do?fmly_id=136

For more detailed technical information about the Voipac PXA270 baseboard components, please refer to the web resources and documents listed below.

Component	Description
Power supply, LM2599S	http://www.national.com/pf/LM/LM2599.html
VGA driver, ADV7125	http://www.analog.com/en/prod/0,,ADV7125,00.html
RTC, DS1339	http://www.maxim-ic.com/ds1339
USB, PCMCIA/CF Power supply, MIC2026	http://www.micrel.com/_PDF/mic2026.pdf

2. Features Description

2.1 User Interfaces

The following user interfaces are available on the Voipac PXA270 baseboard.

Interface	Description
VGA	Maximum resolution 1024x768, 65536 colors (16 bit)
Generic LCD	2x13pin, 2.54mm pin header, active or passive LCD panel
Touch Screen	4-wire resistive touch screen interface
Keyboard & Mouse	2xPS/2 connector
USB	1xUSB Host, 1xUSB Host/Device

2.2 Communication interfaces

Voipac PXA270 baseboard provides the following communication interfaces

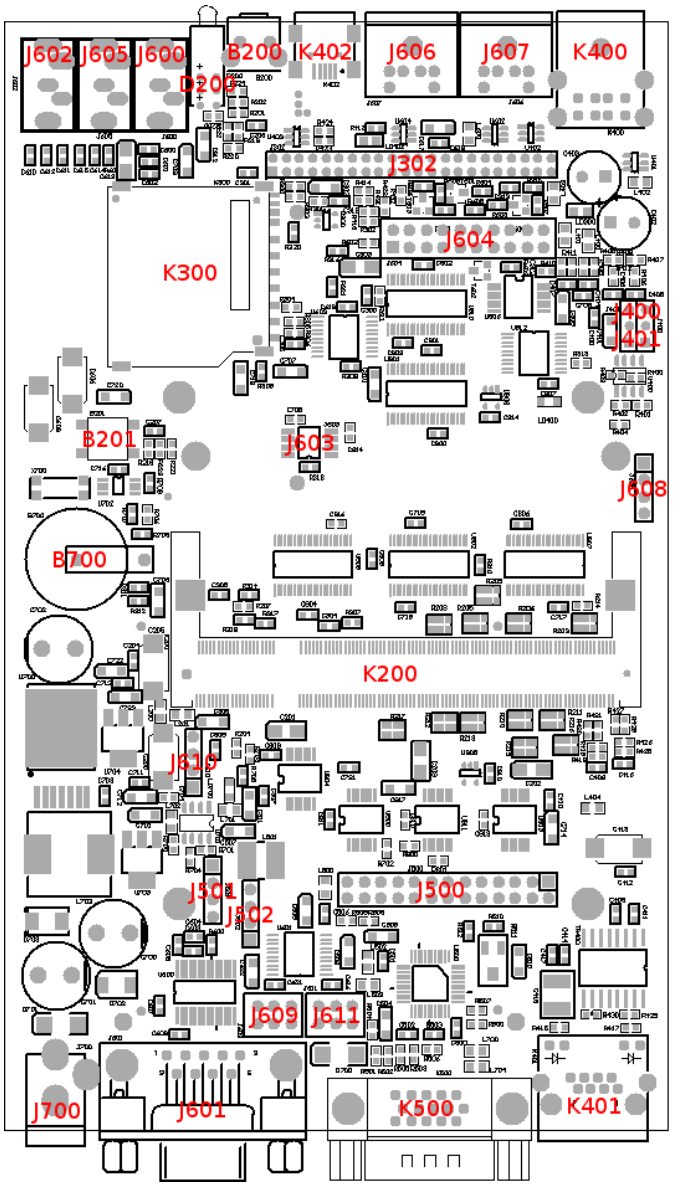
Interface	Description
Ethernet	10/100Mb
USB	1xHost and 1xHost/Device, PC2PC networking supported
Serial	1xRS232 and 2xTTL 3.3V level serial, maximum data rate: 921600bps
Wireless LAN	PCMCIA/CF/SD card or USB wireless
DSL	USB ADSL modem

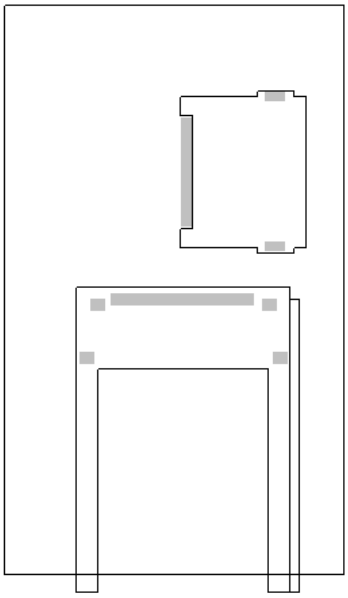
2.3 Extension connectors

Voipac PXA270 baseboard can be further extended by using following interfaces

Interface	Description
PCMCIA/CF	16 bit expansion card
SD/MMC	Serial IO peripherals
IDE	ATA/ATAPI drives or general 16bit VLIO with DMA support
Wireless LAN	GPIO

2.4 Board Layout





Bottom Side

The diagram above shows interfaces layout of Voipac PXA270 module baseboard. Voipac PXA270 module features full 32 bit interfaces to on board SDRAM and ethernet controller. Since not all PXA270 interfaces have dedicated pins some functions could not be used simultaneously. The PCMCIA and CF sockets are on the bottom side.

2.5 Connector and Jumper list

Reference	Type	Description
K200	SODIMM	DDR1 2.5V SODIMM 200pin connector
B200	SW1	Front pannel push button
B201	SW2	Internal push button
D200	3xLED	3xLED HOLDER stacked
J300	PCMCIA	PCMCIA socket
J301	CF	CF socket
J302	IDE	2x22pin, 2mm header
K300	MMC/SD	MMC/SD card socket
J400, J401	USB SWITCH	2x3pin, 2,45mm header
K400	USB HOST	2xUSB-Host stacked
K401	ETHERNET	RJ-45
K402	USB DEVICE	5pin mini USB A
J500	TFT	2x13pin, 2.54mm header
K500	VGA	DSUB15
J501	BACKLIGHT	4pin, 2.54mm header
J502	TOUCH	4pin, 2.54mm header
J600	AUDIO OUT	Jack stereo 3.5mm
J601	RS232	DSUB9 male
J602	AUDIO IN	Jack stereo 3.5mm
J603	JTAG	Molex 47041-0001, board-to-board pitch compression connector
J604	JTAG	2x10pin, 2.54mm header
J605	MIC	Jack stereo 3.5mm
J606	PS/2 MOUSE	DIN6 mini
J607	PS/2 KEYBOARD	DIN6 mini
J608	I2C	4pin, 2.54mm header
J609	BT UART	2x3pin, 2.54mm header
J610	STD UART	4pin, 2.54mm header
J611	SSP	2x3pin, 2.54mm header
J700	POWER	Power jack 5.5/2.1mm
B700	BATT	CR1220 Battery holder

3. Connector Description

This chapter describes the connectors of the Voipac PXA270 baseboard. Some connectors have dedicated functionality, but some like TFT and IDE can be used also for other purposes, like general purpose IO (GPIO) or general expansion bus.

3.1 IO Types Notation

Signal	Description
IN	Digital CMOS input
OUT	Digital CMOS output
IO	Digital CMOS input / output
AIN	Analog input
AOUT	Analog output
AIO	Analog input / output
PWR	Power supply

3.2 Pinout Description

3.2.1 K200 SODIMM (SODIMM 200pin)

Manufacturer: Tyco Electronics, Part No. 6-1473005-1, http://www.tyco.com

Pin#	Pin Name	Type	Description
1	MIC_IN	AIN	Microphone Input
2	AD3	AIN	AD Converter Input 3
3	MIC_GND	PWR	Microphone Ground
4	AD2	AIN	AD Converter Input 2
5	LINEIN_L	AIN	Line Input (Left Channel)
6	AD1	AIN	AD Converter Input 1
7	LINEIN_R	AIN	Line Input (Right Channel)
8	AD0	AIN	AD Converter Input 0
9	VSSA_AUDIO	PWR	Audio Codec Ground
10	VDDA_AUDIO	PWR	Audio Codec Power supply (connect to 3.3V)
11	VSSA_AUDIO	PWR	Audio Codec Ground
12	VDDA_AUDIO	PWR	Audio Codec Power supply (connect to 3.3V)
13	HEADPHONE_GND	PWR	Headphone Ground

Pin#	Pin Name	Type	Description
14	TSPX	AIO	4wire Resistive Touch Panel (X Plus Terminal)
15	HEADPHONE_L	AOUT	Headphone Output (Left Channel)
16	TSMX	AIO	4wire Resistive Touch Panel (X Minus Terminal)
17	HEAPHONE_R	AOUT	Headphone Output (Right Channel)
18	TSPY	AIO	4wire Resistive Touch Panel (Y Plus Terminal)
19	GPIO46/STD_RXD	IN	Receive Pin for Standard UART
20	TSMY	AIO	4wire Resistive Touch Panel (Y Minus Terminal)
21	GPIO47/STD_TXD	OUT	Transmit Pin for Standard UART
22	VDD_FAULT	IN	VDD Fault: This input signals that the main power source is going out of regulation. nVDD_FAULT causes the PXA27x processor to enter sleep mode or, if PMCR[VIDAE] is set, forces an imprecise-data abort, which cannot be masked. nVDD_FAULT is ignored after a wake-up event until the power supply timer completes (approximately 10 ms).
23	GPIO40/FF_DTR	OUT	Full-Function UART Data-Terminal-Ready
24	BATT_FAULT	IN	Main Battery Fault: This input signals that the main battery is low or removed. Assertion causes the PXA27x processor to enter sleep mode or, if PMCR[BIDAE] is set, forces an imprecise-data abort, which cannot be masked. The PXA27x processor does not recognize a wake-up event while this signal is asserted.
25	GPIO100/FF_CTS	IN	Full-Function UART Clear-to-Send
26	nRESET_IN	IN	Reset: This active-low, level-sensitive input starts the processor from the reset vector at address 0. Assertion causes the current instruction to terminate abnormally and causes a reset. When nRESET is driven high, the processor starts execution from address 0. nRESET must remain low until the power supply is stable and the internal 13-MHz oscillator has stabilized.
27	GPIO27/FF_RTS	OUT	Full-Function UART Request-to-Send
28	GPIO11		
29	GPIO33/FF_DSR	IN	Full-Function UART Data-Set-Ready
30	GPIO16		
31	GPIO10/FF_DCD	IN	Full-Function UART Data-Carrier-Detect
32	GPIO44/BT_CTS	IN	Bluetooth UART Clear-to-Send
33	GPIO34/FF_RXD	IN	Full-Function UART Receive Data
34	GPIO45/BT_RTS	OUT	Bluetooth UART Request-to-Send
35	GPIO39/FF_TXD	OUT	Full-Function UART Transmit Data
36	GPIO42/BT_RXD	IN	Bluetooth UART Receive Data
37	GPIO38/FF_RI	IN	Full-Function UART Ring Indicator
38	GPIO43/BT_TXD	OUT	Bluetooth UART Transmit Data
39	GND	PWR	Ground
40	+3V3	PWR	Main power supply (connect to 3.3V)
41	GND	PWR	Ground
42	+3V3	PWR	Main power supply (connect to 3.3V)
43	GPIO0		
44	GPIO77/L_BIAS	OUT	LCD Bias Drive: AC bias that signals the LCD display module to switch the polarity of the power supplies to the row and column axis of the screen to counteract DC offset. In active (TFT) mode, it is used as the output enable to signal when data should be latched from the data pins using the pixel clock.
45	GPIO1		

Pin#	Pin Name	Type	Description
46	GPIO65/LDD07	IO	LCD Display Data 7
47	GPIO32/MMCLK	OUT	MMC and SD/SDIO Card Bus Clock
48	GPIO67/LDD09	IO	LCD Display Data 9
49	GPIO109/MMDAT1	IO	MMC and SD/SDIO Data 1
50	GPIO69/LDD11	IO	LCD Display Data 11
51	GPIO110/MMDAT2/MMCS0	IO	SD/SDIO Data 2 or MMC Chip Select 0
52	GPIO70/LDD12	IO	LCD Display Data 12
53	GPIO111/MMDAT3/MMCS1	IO	SD/SDIO Data 3 or MMC Chip Select 1
54	GPIO71/LDD13	IO	LCD Display Data 13
55	GPIO19/L_CS	OUT	LCD Chip Select: Chip select signal for LCD panels with an internal frame buffer.
56	GPIO76/L_PCLK_WR	OUT	LCD Pixel Clock: Pixel clock used by the LCD display module to clock the pixel data into the line shift register. In passive mode, the pixel clock toggles only when valid data is available on the data pins. In active mode, the pixel clock toggles continuously, and the AC bias pin is used as an output to signal when data is valid on the LCD data pins. This pin also functions as a write signal for LCD panels with an internal frame buffer.
57	GPIO86/LDD16	IO	LCD Display Data 16
58	GPIO61/LDD03	IO	LCD Display Data 3
59	GPIO12		
60	GPIO60/LDD02	IO	LCD Display Data 2
61	GPIO87/LDD17	IO	LCD Display Data 17
62	GPIO66/LDD08	IO	LCD Display Data 8
63	GPIO14		
64	GPIO73/LDD15	IO	LCD Display Data 15
65	GPIO106		
66	GPIO72/LDD14	IO	LCD Display Data 14
67	GPIO17		
68	GPIO75/L_LCLK_A0	OUT	LCD Line Clock: Indicates the start of a new line. Also referred to as HSync (or horizontal synchronization) for active panels. For LCDs with an internal frame buffer, this signal indicates a command or data transaction.
69	GPIO20		
70	GPIO59/LDD01	IO	LCD Display Data 1
71	GPIO81		
72	GPIO63/LDD05	IO	LCD Display Data 5
73	GPIO52		
74	GPIO68/LDD10	IO	LCD Display Data 10
75	GPIO53		
76	GPIO58/LDD00	IO	LCD Display Data 0
77	GPIO82		
78	GPIO62/LDD04	IO	LCD Display Data 4
79	GPIO83		
80	GPIO64/LDD06	IO	LCD Display Data 6
81	GPIO84		

Pin#	Pin Name	Type	Description
82	GPIO74/L_FCLK_RD	OUT	LCD Frame Clock: Frame clock used by the LCD display module to signal the start of a new frame of pixels that resets the line pointers to the top of the screen. This pin is also the vertical synchronization signal for active (TFT) displays. This pin is the read signal during reads from a panel with an internal frame buffers.
83	GND	PWR	Ground
84	+3V3	PWR	Main power supply (connect to 3.3V)
85	GPIO107		
86	GPIO24/SSPFRM	IO	Synchronous Serial Port 1 Frame: The serial frame sync can be configured as an output (master-mode) or an input (slave-mode).
87	nRESET_OUT	OUT	Reset Out: Asserted when nRESET is asserted, it deasserts after nRESET is deasserted but before the first instruction fetch occurs. nRESET_OUT is asserted during power-on, hardware, watchdog, and sleep-exit resets. It is configurable for GPIO reset.
88	GPIO23/SSPCLK	IO	Synchronous Serial Port 1 Clock: The serial bit-clock can be configured as an output (master-mode) or an input (slave-mode).
89	nWE	O	Memory Write Enable: Connect to the write enables of SDRAM and static memory devices.
90	GPIO26/SSPRXD	IN	Synchronous Serial Port 1 Receive Data: Serial data latched using the bit-clock.
91	nOE	O	Memory Output Enable: Connect to the output enables of static memory devices to control data bus drivers.
92	GPIO25/SSPTXD	OUT	Synchronous Serial Port 1 Transmit Data: Serial data driven out synchronously with the bit-clock.
93	RDnWR	OUT	Read/Write: Indicates that the current transaction is a read (high) or a write (low)
94	GPIO85/nPCE1	OUT	PC Card Enable 1: Selects a PC Card. nPCE1 enables the low byte lane.
95	RDY(GPIO18)	IN	Variable Latency I/O Ready Pin: An external variable-latency I/O (VLIO) device asserts RDY when it is ready to transfer data.
96	GPIO54/nPCE2	OUT	PC Card Enable 2: Selects a PC Card. nPCE2 enables the high byte lane.
97	GPIO48/nPOE	OUT	PC Card Output Enable: Output enable for reads from PC Card memory and PC Card attribute space.
98	GPIO55/nPREG	OUT	PC Card Register Select: Functions as address bit 26 to select register space (I/O or attribute) or memory space. Has the same timing as the address bus.
99	nPWE(GPIO49)	OUT	PC Card Write Enable: Enables writes to PC Card memory and PC Card attribute space. Also serves as the write enable signal for variable-latency I/O.
100	GPIO104/PSKTSEL	OUT	PC Card Socket Select: Used by external steering logic to route control, address, and data signals to one of the two PC Card sockets. Active-low output enable that can be used as nOE for the data transceivers. The signal has the same timing as the address bus. In a single socket solution: 0 = Output enable selected 1 = Output enable not selected In a dual socket solution, the socket select: 0 = Socket 0 selected 1 = Socket 1 selected
101	GPIO51/nPIOW	OUT	PC Card I/O Write: Asserted for writes to PC Card I/O space.
102	GPIO56/nPWAIT	IN	PC Card Wait: Driven low by the PC Card to insert wait states, which extend transfers to and from the PXA27x processor.
103	GPIO50/nPIOR	OUT	PC Card I/O Read: Asserted for reads from PC Card I/O space.
104	GPIO57/nIOIS16	IN	I/O Select 16: Input from the PC Card indicating that the data bus: 0 = Data bus is 8 bits wide 1 = Data bus is 16 bits wide
105	GPIO15/nCS1	OUT	Static Chip Select 1: Physical Address 0x04000000

Pin#	Pin Name	Type	Description
			Static Chip Selects: Chip selects to static memory devices such as ROM and flash, individually programmable in the memory configuration registers. nCS<5:0> can be used with variable-latency I/O devices. nCS<3:0> can be used with synchronous flash.
106	GPIO80/nCS4	OUT	Static Chip Select 4: Physical Address 0x10000000
107	GPIO79/nCS3	OUT	Static Chip Select 3: Physical Address 0x0C000000
108	+3V3	PWR	Main power supply (connect to 3.3V)
109	GND	PWR	Ground
110	MA08	OUT	MA[25:0] Memory Address Bus: Address for external memory accesses.
111	MA00	OUT	
112	MA09	OUT	
113	MA01	OUT	
114	MA10	OUT	
115	MA02	OUT	
116	MA11	OUT	
117	MA03	OUT	
118	MA12	OUT	
119	MA04	OUT	
120	MA13	OUT	
121	MA05	OUT	
122	MA14	OUT	
123	MA06	OUT	
124	MA15	OUT	
125	MA07	OUT	
126	DQM0	OUT	DQM Data Byte Mask Control 0: Corresponds to MD<7:0>.
127	GPIO36/OTG_VBUS_EN		
128	DQM1	OUT	DQM Data Byte Mask Control 1: Corresponds to MD<15:8>.
129	GPIO89/USBH1_PEN	OUT	USB Host Power Enable: Controls power IC for USB host port.
130	DQM2	OUT	DQM Data Byte Mask Control 2: Corresponds to MD<23:16>.
131	GPIO88/USBH1_OC	IN	USB Host Power Indicator: Over-current indicator from USB power IC for USB host port.
132	DQM3	OUT	DQM Data Byte Mask Control 3: Corresponds to MD<31:24>.
133	GPIO37/OTG_VBUS_PULSE		
134	MA25	OUT	
135	GPIO35/OTG_SRP_DETECT		
136	MA24	OUT	
137	GPIO41/OTG_ID		
138	MA23	OUT	
139	USBH_P	IO	USB Host Positive Line: Differential signal connects to the USB host interface.
140	MA22	OUT	
141	USBH_N	IO	USB Host Negative Line: Differential signal connects to the USB host interface.
142	MA21	OUT	

Pin#	Pin Name	Type	Description
143	USBC_P	IO	USB Client Positive Line: Differential signal connects to the USB client interface.
144	MA20	OUT	
145	USBC_N	IO	USB Client Negative Line: Differential signal connects to the USB client interface.
146	MA19	OUT	
147	GND	PWR	Ground
148	+3V3	PWR	Main power supply (connect to 3.3V)
149	MD00	IO	MD[31:0] Memory Data Bus: Data bus to and from external memory devices.
150	MD16	IO	
151	MD01	IO	
152	MD17	IO	
153	MD02	IO	
154	MD18	IO	
155	MD03	IO	
156	MD19	IO	
157	MD04	IO	
158	MD20	IO	
159	MD05	IO	
160	MD21	IO	
161	MD06	IO	
162	MD22	IO	
163	MD07	IO	
164	MD23	IO	
165	MD08	IO	
166	MD24	IO	
167	MD09	IO	
168	MD25	IO	
169	MD10	IO	
170	MD26	IO	
171	MD11	IO	
172	MD27	IO	
173	MD12	IO	
174	MD28	IO	
175	MD13	IO	
176	MD29	IO	
177	MD14	IO	
178	MD30	IO	
179	MD15	IO	
180	MD31	IO	
181	GND	PWR	Ground
182	+3V3	PWR	Main power supply (connect to 3.3V)

Pin#	Pin Name	Type	Description
183	nETH_LINK_ACT	OUT	Ethernet Activity Indicator
184	MA18	OUT	
185	nETH_SPEED100	OUT	Ethernet Speed Indicator
186	MA17	OUT	
187	ETH_TXO-	OUT	Ethernet TX Differential Output (minus)
188	MA16	OUT	
189	ETH_TXO+	OUT	Ethernet TX Differential Output (plus)
190	GPIO112/MMCMD	IO	MMC and SD/SDIO command and response tokens.
191	ETH_AGND	PWR	Ethernet Analog Ground
192	GPIO92/MMDAT0	IO	MMC and SD/SDIO Data 0
193	ETH_RXI-	IN	Ethernet RX Differential Input (minus)
194	GPIO118/I2C_DATA	IO	I2C Data: Serial data/address bus.
195	ETH_RXI+	IN	Ethernet RX Differential Input (plus)
196	GPIO117/I2C_CLK	IO	I2C Clock: Serial clock.
197	GND	PWR	Ground
198	+3V3	PWR	Main power supply (connect to 3.3V)
199	GND	PWR	Ground
200	+3V3	PWR	Main power supply (connect to 3.3V)

3.2.2 B200 SW1 (front pannel)

The front panel push button switch SW1 can be configured to function as GPIO1 or RESET signal by an assembly option. By default it is assembled to function as GPIO1 signal.

SW1 Function	R218	R222	Description
GPIO1	0R	open	
RESET	open	0R	

3.2.3 B201 SW2 (internal)

The internal push button switch SW2 can be configured to function as GPIO1 or RESET signal by an assembly option. By default it is assembled to function as RESET.

SW2 Function	R219	R223	Description
GPIO1	open	0R	
RESET	0R	open	

3.2.4 D200 3xLED HOLDER

The 3xLED holder has LED2 (middle) connected to GPIO15 for general purpose use by customer application. The LED colors can vary.

Function	Color	Position	Description
POWER	GREEN	TOP	Indicates the Power supply is present
USER	ORANGE	MIDDLE	GPIO15
HDD	RED	BOTTOM	HDD drive activity

3.2.5 J300 PCMCIA

Manufacturer: AVX , Part No. 315027068130871, http://www.kyocera-elco.com

The hardware supported card detect function is implemented, including hot plug feature also. Power enable signal is generated by GPIO107.

Pin#	Pin Name	Type	Description
1	GND	PWR	Ground
2	D[3]	IO	D[15:0] PC Card Data Bus
3	D[4]	IO	
4	D[5]	IO	
5	D[6]	IO	
6	D[7]	IO	
7	PCE1	OUT	PC Card Enable 1: Selects a PC Card
8	A[10]	OUT	A[10:0] PC Card Address Bus
9	POE	OUT	PC Card Output Enable
10	A[11]	OUT	
11	A[9]	OUT	
12	A[8]	OUT	
13	A[13]	OUT	
14	A[14]	OUT	
15	PWE	OUT	PC Card Write Enable
16	PRDY	IN	PC Card Ready
17	VCC	PWR	Power supply (connected to 3.3V when GPIO107 is low)
18	VPP1	PWR	
19	A[16]	OUT	
20	A[15]	OUT	
21	A[12]	OUT	
22	A[7]	OUT	

Pin#	Pin Name	Type	Description
23	A[6]	OUT	
24	A[5]	OUT	
25	A[4]	OUT	
26	A[3]	OUT	
27	A[2]	OUT	
28	A[1]	OUT	
29	A[0]	OUT	
30	D[0]	IO	
31	D[1]	IO	
32	D[2]	IO	
33	PIOIS16	IN	I/O Select 16: Input from the PC Card indicating data bus width
34	GND	PWR	
35	GND	PWR	
36	CD1	IN	PC Card Detect 1: Logic OR function of CD1 and CD2 signal is connected to GPIO17
37	D[11]	IO	
38	D[12]	IO	
39	D[13]	IO	
40	D[14]	IO	
41	D[15]	IO	
42	PCE2	OUT	PC Card Enable 2: Selects a PC Card
43	VS1	IN	PC Card Voltage Select 1: Not used
44	PIOR	OUT	PC Card I/O Read
45	PIOW	OUT	PC Card I/O Write
46	A[17]	OUT	
47	A[18]	OUT	
48	A[19]	OUT	
49	A[20]	OUT	
50	A[21]	OUT	
51	VCC	PWR	Power supply (connected to 3.3V)
52	VPP2	PWR	
53	A[22]	OUT	
54	A[23]	OUT	
55	A[24]	OUT	
56	A[25]	OUT	
57	VS2	IN	PC Card Voltage Select 2: Not used
58	PRST	OUT	PC Card Reset: Signal is generated by GPIO16 and is shared by IDE interface
59	PWAIT	IN	PC Card Wait
60	INPACK	IN	
61	PREG	OUT	PC Card Register Select
62	PBVD2	IN	PC Card Battery Voltage Detect 2: Not used

Pin#	Pin Name	Type	Description
63	PBVD1	IN	PC Card Battery Voltage Detect 1: Not used
64	D[8]	IO	
65	D[9]	IO	
66	D[10]	IO	
67	CD2	IN	PC Card Detect 2
68	GND	PWR	Ground

3.2.6 J301 CF

Manufacturer: Molex , Part No. 67155-0002, http://www.molex.com

The hardware supported card detect function is implemented, but not hot plug feature.

Pin#	Pin Name	Type	Description
1	GND	PWR	Ground
2	D[3]	IO	D[15:0] PC Card Data Bus
3	D[4]	IO	
4	D[5]	IO	
5	D[6]	IO	
6	D[7]	IO	
7	PCE1	OUT	PC Card Enable 1: Selects a PC Card
8	A[10]	OUT	A[10:0] PC Card Address Bus
9	POE	OUT	PC Card Output Enable
10	A[9]	OUT	
11	A[8]	OUT	
12	A[7]	OUT	
13	VCC	PWR	Power supply (connected to 3.3V)
14	A[6]	OUT	
15	A[5]	OUT	
16	A[4]	OUT	
17	A[3]	OUT	
18	A[2]	OUT	
19	A[1]	OUT	
20	A[0]	OUT	
21	D[0]	IO	
22	D[1]	IO	
23	D[2]	IO	
24	PIOIS16	IN	I/O Select 16: Input from the PC Card indicating data bus width
25	CD1	IN	PC Card Detect 1: Logic OR function of CD1 and CD2 signal is connected to GPIO17
26	CD2	IN	PC Card Detect 2
27	D[11]	IO	

Pin#	Pin Name	Type	Description
28	D[12]	IO	
29	D[13]	IO	
30	D[14]	IO	
31	D[15]	IO	
32	PCE2	OUT	PC Card Enable 2: Selects a PC Card
33	VS1	IN	PC Card Voltage Select 1: Not used
34	PIOR	OUT	PC Card I/O Read
35	PIOW	OUT	PC Card I/O Write
36	PWE	OUT	PC Card Write Enable
37	PRDY	IN	PC Card Ready
38	VCC	PWR	Power supply (connected to 3.3V)
39	CSEL	IN	PC Card Cable Select: Connected to GND
40	VS2	IN	PC Card Voltage Select 2: Not used
41	PRST	OUT	PC Card Reset: Signal is generated by GPIO16 and is shared by IDE interface
42	PWAIT	IN	PC Card Wait
43	INPACK	IN	
44	PREG	OUT	PC Card Register Select
45	PBVD2	IN	PC Card Battery Voltage Detect 2: Not used
46	PBVD1	IN	PC Card Battery Voltage Detect 1: Not used
47	D[8]	IO	
48	D[9]	IO	
49	D[10]	IO	
50	GND	PWR	Ground

3.2.7 J302 IDE (2x22pin, 2mm header)

The hardware supported MWDMA2 mode is implemented.

Pin#	Pin Name	Type	Description
1	nRESET	OUT	Reset: Signal is generated by GPIO16(active high) and is shared by CF interface
2	GND	PWR	Ground
3	DD7	IO	DD[15:0] Data Bus
4	DD8	IO	
5	DD6	IO	
6	DD9	IO	
7	DD5	IO	
8	DD10	IO	
9	DD4	IO	
10	DD11	IO	
11	DD3	IO	
12	DD12	IO	

Pin#	Pin Name	Type	Description
13	DD2	IO	
14	DD13	IO	
15	DD1	IO	
16	DD14	IO	
17	DD0	IO	
18	DD15	IO	
19	GND	PWR	Ground
20	KEY		
21	DMARQ	IN	DMA Request
22	GND	PWR	Ground
23	nDIOW	OUT	I/O Write Strobe
24	GND	PWR	Ground
25	nDIOR	OUT	I/O Read Strobe
26	GND	PWR	Ground
27	IORDY	IN	I/O Ready
28	CSEL	IN	Cable select, connected to GND
29	nDMACK	OUT	DMA Acknowledge
30	GND	PWR	Ground
31	INTRQ	IN	Interrupt Request
32	nIOCS16	IN	IO Chip Select 16: Not used
33	DA1	OUT	DA[2:0]: Address Bus
34	PDIAG	IO	Passed Diagnostics: Not used
35	DA0	OUT	
36	DA2	OUT	
37	nCS0	OUT	nCS[1:0] Chip Select
38	nCS1	OUT	
39	nACTIVE	OUT	Led driver
40	GND	PWR	Ground
41	VCC	PWR	Power supply (connected to +5V)
42	VCC	PWR	Power supply (connected to +5V)
43	GND	PWR	Ground
44	nTYPE	OUT	Type (0=ATA): Not used

3.2.8 K300 MMC/SD

Manufacturer: Multicomp, Part No. SD SDCMF-10915W010, http://www.farnell.com

The hardware supported card detect feature is implemented by GPIO53 and software write protect detection using GPIO52.

Pin#	Pin Name	Type	Description
1	MMDAT[3]	IO	SD/SDIO Data 3 or MMC Chip Select 1
2	MMCMD	IN	MMC and SD/SDIO command and response tokens.
3	GND	PWR	Ground
4	VCC	PWR	Power supply (connected to +3.3V)
5	MMCLK	IN	MMC and SD/SDIO Card Bus Clock
6	GND	PWR	Ground
7	MMDAT[0]	IO	MMC and SD/SDIO Data 0
8	MMDAT[1]	IO	MMC and SD/SDIO Data 1
9	MMDAT[2]	IO	SD/SDIO Data 2 or MMC Chip Select 0
10	CD	IN	MMC/SD Card Detect, connected to GPIO53
11	WP	IN	MMC/SD Write Protect, connected to GPIO52

3.2.9 J400, J401 USB SWITCH *(2x3pin, 2,45mm header)*

The Voipac PXA270 baseboard offers a dedicated USB Host as well as a shared USB Host/Client. The configuration of the shared USB channel is selected through the jumpers setting J400 and J401. USB Device detect feature is implemented by GPIOxx.

Function	J400	J401	Description
2x USB HOST	2-3	2-3	
USB HOST + mini USB 2.0 DEVICE	1-2	1-2	Active USB HOST is top

3.2.10 K400 USB HOST *(2 x USB-Host stacked)*

Pin#	Pin Name	Type	Description
A1	USB_AVCC	PWR	Power supply (connected to +5V when GPIOxx is low)
A2	USBH1_NEXT	IO	USB Host Data1-
A3	USBH1_PEXT	IO	USB Host Data1+
A4	GND	PWR	Ground
B1	USB_AVCC	PWR	Power supply (connected to +5V when GPIOxx is low)
B2	USBH2_NEXT	IO	USB Host Data2-
B3	USBH2_PEXT	IO	USB Host Data2+
B4	GND	PWR	Ground

3.2.11 K401 ETHERNET (RJ-45)

Pin#	Pin Name	Type	Description
1	TX+	OUT	ETH Transmit+
2	TX-	OUT	ETH Transmit-
3	RX+	IN	ETH Receive+
4	LAN45+	PWR	Power over LAN cable supply (7-37 V)
5	LAN45+	PWR	
6	RX-	IN	ETH Receive-
7	LAN78	PWR	Power over LAN Ground
8	LAN78	PWR	

3.2.12 K402 USB DEVICE (5pin mini USB A)

Pin#	Pin Name	Type	Description
1	USB_AVCC	PWR	External Power supply (connected to +5V when device plugged in)
2	USBC_NEXT	IO	USB Device Data-
3	USBC_PEXT	IO	USB Device Data+
4	USB_ID	IN	USB ID: Not used
5	GND	PWR	Ground

3.2.13 J500 TFT (2x13pin, 2.54mm header)

Pin#	Pin Name	Type	Description
1	LCLK		Horizontal Sync (Line Clock)
2	PCLK		Pixel Clock
3	LDD12		LCD Display Data LDD[17:0]
4	FCLK		Vertical Sync (Frame Clock)
5	LDD14		
6	LDD13		
7	LDD16		
8	LDD15		
9	LDD6		
10	LDD17		
11	LDD8		
12	LDD7		
13	LDD10		
14	LDD9		
15	LDD0		
16	LDD11		

Pin#	Pin Name	Type	Description
17	LDD2		
18	LDD1		
19	LDD4		
20	LDD3		
21	nLON		Display on (connected to GPIO83)
22	LDD5		
23	+3V3		Display power supply (connected to +3.3V)
24	+5V		Display power supply (connected to +5V)
25	GND		Ground
26	VCON		Display contrast, adjustable by trimmer R511

3.2.14 K500 VGA (DSUB15)

Pin#	Pin Name	Type	Description
1	RED	AOUT	Red Video (75Ω, 0.7 Vpp)
2	GREEN	AOUT	Green Video (75Ω, 0.7 Vpp)
3	BLUE	AOUT	Blue Video (75Ω, 0.7 Vpp)
4	NC		
5	GND	PWR	Ground
6	RGND	PWR	Red Ground
7	GGND	PWR	Green Ground
8	BGND	PWR	Blue Ground
9	KEY		
10	SGND	PWR	Sync Ground
11	NC		
12	NC		
13	LCLK	OUT	Horizontal Sync (Line Clock)
14	FCLK	OUT	Vertical Sync (Frame Clock)
15	NC		

3.2.15 J501 BACKLIGHT (4pin, 2.54mm header)

Pin#	Pin Name	Type	Description
1	+5V	PWR	Backlight power supply (connected to +5V)
2	GND	PWR	Ground
3	BKLON	OUT	Backlight on (connected to GPIO81)
4	GND	PWR	Ground

3.2.16 J502 *TOUCH* (4pin, 2.54mm header)

Pin#	Pin Name	Type	Description
1	TSPX	AIO	4wire Resistive Touch Panel (X Plus Terminal)
2	TSPY	AIO	4wire Resistive Touch Panel (Y Plus Terminal)
3	TSMX	AIO	4wire Resistive Touch Panel (X Minus Terminal)
4	TSMY	AIO	4wire Resistive Touch Panel (Y Minus Terminal)

3.2.17 J600 *AUDIO OUT* (Jack stereo 3.5mm)

Pin#	Pin Name	Type	Description
1	LEFT	AOUT	Line out left channel
2	RIGHT	AOUT	Line out right channel
3	AGND	PWR	Audio Ground

3.2.18 J601 *RS232* (DSUB9 male)

Pin#	Pin Name	Type	Description
1	FF_DCD	IN	Carrier Detect
2	FF_RXD	IN	Receive Data
3	FF_TXD	OUT	Transmit Data
4	FF_DTR	OUT	Data Terminal Ready
5	GND	PWR	Ground
6	FF_DSR	IN	Data Set Ready
7	FF_RTS	OUT	Request to Send
8	FF_CTS	IN	Clear to Send
9	FF_RI	IN	Ring Indicato

3.2.19 J602 *AUDIO IN* (Jack stereo 3.5mm)

Pin#	Pin Name	Type	Description
1	LEFT	AIN	Line in left channel
2	RIGHT	AIN	Line in right channel
3	AGND	PWR	Audio Ground

3.2.20 J603 JTAG (board-to-board pitch compression connector)

Manufacturer: Molex , Part No. 47041-0001, http://www.molex.com

Pin#	Pin Name	Type	Description
1	+3V3	PWR	Supply power to power up JTAG logic
2	GND	PWR	Ground
3	TMS	IN	JTAG mode select
4	nTRST	IN	JTAG reset
5	TCK	IN	JTAG clock
6	TDO	OUT	JTAG Data output
7	TDI	IN	JTAG Data input
8	nSRST	IN	System Reset

3.2.21 J604 JTAG (2x10pin, 2.54mm header)

Pin#	Pin Name	Type	Description
1	VREF	PWR	Reference JTAG Interface Voltage (connected to +3.3V)
2	VDD	PWR	Power supply (connected to +3.3V)
3	nTRST	IN	JTAG reset
4	VSS	PWR	Ground
5	TDI	IN	JTAG Data input
6	VSS	PWR	Ground
7	TMS	IN	JTAG mode select
8	VSS	PWR	Ground
9	TCK	IN	JTAG clock
10	VSS	PWR	Ground
11	RTCK	OUT	Not used
12	VSS	PWR	Ground
13	TDO	OUT	JTAG Data output
14	VSS	PWR	Ground
15	nSRST	IN	System Reset
16	VSS	PWR	Ground
17	DBGRQ	IN	Not used
18	VSS	PWR	Ground
19	DBGACK	OUT	Not used
20	VSS	PWR	Ground

3.2.22 J605 *MIC* (Jack stereo 3.5mm)

Pin#	Pin Name	Type	Description
1	MICP	AOUT	Microphone Input (pulled up to +3.3V by 1kΩ)
2	NC		
3	AGND	PWR	Audio Ground

3.2.23 J606 *PS/2 MOUSE* (DIN6 mini)

Pin#	Pin Name	Type	Description
1	MS_DATA	IO	Mouse Data
2	NC		
3	GND	PWR	Ground
4	VCC	PWR	Power supply (connected to +5V)
5	MS_CLK	OUT	Mouse Clock
6	NC		

3.2.24 J607 *PS/2 KEYBOARD* (DIN6 mini)

Pin#	Pin Name	Type	Description
1	KBD_DATA	IO	Keyboard Data
2	NC		
3	GND	PWR	Ground
4	VCC	PWR	Power supply (connected to +5V)
5	KBD_CLK	OUT	Keyboard Clock
6	NC		

3.2.25 J608 *I2C* (4pin, 2.54mm header)

Pin#	Pin Name	Type	Description
1	SCL	IO	I2C Bus Clock
2	SDA	IO	I2C Bus Data
3	+3.3V	PWR	Power supply (connected to +3.3V)
4	GND	PWR	Ground

3.2.26 J609 BT UART (2x3pin, 2.54mm header)

Pin#	Pin Name	Type	Description
1	BT_CTS	IN	Clear to Send
2	BT_TXD	OUT	Transmit Data
3	BT_RTS	OUT	Request to Send
4	+3.3V	PWR	Power supply (connected to +3.3V)
5	BT_RXD	IN	Receive Data
6	GND	PWR	Ground

3.2.27 J610 STD UART (4pin, 2.54mm header)

Pin#	Pin Name	Type	Description
1	+3.3V	PWR	Power supply (connected to +3.3V)
2	STD_TXD	OUT	Transmit Data
3	STD_RXD	IN	Receive Data
4	GND	PWR	Ground

3.2.28 J611 SSP (2x3pin, 2.54mm header)

Pin#	Pin Name	Type	Description
1	SSP_FRM	IO	Synchronous Serial Port Frame: The serial frame sync can be configured as an output (master-mode) or an input (slave-mode).
2	SSP_RXD	IN	Synchronous Serial Port Receive Data: Serial data latched using the bit-clock.
3	SSP_CLK	IO	Synchronous Serial Port Clock: The serial bit-clock can be configured as an output (master-mode) or an input (slave-mode).
4	+3.3V	PWR	Power supply (connected to +3.3V)
5	SSP_TXD	OUT	Synchronous Serial Port Transmit Data: Serial data driven out synchronously with the bit-clock.
6	GND	PWR	Ground

3.2.29 J700 POWER (Power jack 5.5/2.1mm)

Pin#	Pin Name	Type	Description
1	VCC	PWR	Power supply (input voltage 7-37V DC)
2	GND	PWR	Ground

3.2.30 B700 BATT (CR1220 Battery holder)

Pin#	Pin Name	Type	Description
1	BATP	PWR	Battery Positive
2	BATN	PWR	Ground

4. Technical Specifications

4.1 Input Voltage

Voipac PXA270 baseboard on board 5V switching power supply has input voltage ranging from 7V to 37V. Maximum output current of the regulator is 3A thus limiting baseboard, module and all connected peripherals to 15W maximum power consumption.

4.2 Mechanical

Dimmensions	Width	Height	Length	Unit
PCB	105	1.5	168	mm
Aluminium Case	112	30	175	mm

4.3 Temperature Range

Symbol	Description	Min	Max	Unit
T_AMB	Operating temperature range	-25	85	°C

4.4 RoHS and WEEE Compliance

All of the products designed and manufactured by Voipac Technologies are classified as Electrical and Electronic Equipment (EEE) under the Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment 2002/95/EC (RoHS). To comply with the RoHS directive, the restricted use of Lead (Pb), Mercury (Hg), Cadmium (Cd), Hexavalent Chromium (Cr 6+), Polybrominated Biphenyls (PBB) and Polybrominated Diphenyl Ethers (PBDE) must be ensured. Voipac Technologies guarantees that products ordered after July 1, 2006 are assembled in full compliance with the RoHS directive from the European Parliament and Counsel. The company procedures also complies with the Waste Electrical and Electronic Equipment Directive 2002/96/EC (WEEE) .

5. Support

All the relevant communication should be executed via e-mails preferably. Response time is up to 48 hours, except state holidays and weekends. Voipac Technologies working hours are: 8:00 - 17:00, Monday – Friday.

To claim warranty and RMA number assignment, please fill in this protocol/problem description form and send it to: reclamations@voipac.com.
Board warranty without the protocol/problem description will not be processed.
For more information, see our General Terms and Conditions.

Besides the free-of-charge support, we provide support for your new designs when it comes to the special drivers for the peripherals not included in the Voipac development kits, design of your own base boards, prototyping, or even new products development, please contact: support@voipac.com for more info.

By registering on Voipac`s Internet Customer Details site, you will be granted to access the Voipac Ticketing System, where you can post support request tickets and receive e-mail notifications upon any change of your ticket's status.

6. Distributors

Austria

KDS Handelsgesellschaft mBH
Rienoesslgasse 22/11
1040 Vienna, Austria
Phone: 0043 1 7260408
Fax: 0043 1 546804983
E-mail: office@kds.at

Ukraine

Technotrade Ltd
Polupanova 10
04114 Kiev, Ukraine
Phone / Fax:
0038 44 5024655 (-77)
0038 44 2369055 (-57)
E-mail: voipac@tit.kiev.ua

Italy

Adelsy srl
via J. Lennon 6
40057 Cadriano di Granarolo dell'Emilia, Italia
Phone: 0039 51 763069
Fax: 0039 51 763073
E-mail: Info@Adelsy.it

Italy

Dofware s.r.l.
C.so IV Novembre, 7
10036 Settimo Torinese, Italia
Phone: 0039 011 569.24.45
Fax: 0039 011 995.17.34
E-mail: Info@dofware.com

Spain & Portugal

Monolitic, s.a.
Avda Vallcarca 78-80
08023 Barcelona, Spain
Phone: 0034 932859292
Fax: 0034 932841193
E-mail: monolitic@monolitic.com

Spain & Portugal

MATRIX ELECTRONICA
C/Alejandro Sanchez, 109
28019 Madrid, Spain
Phone: +34 902 19 81 46
Fax: +34 902 99 54 14
E-mail: matrix@matrix.es

The Netherlands

Alcom Electronics bv
Rivium 1e straat 52
2909 LE Capelle ad IJssel
Tel: +31.10.288.2500
Fax: +31.10.288.2525
E-mail: info@alcom.nl

Belgium

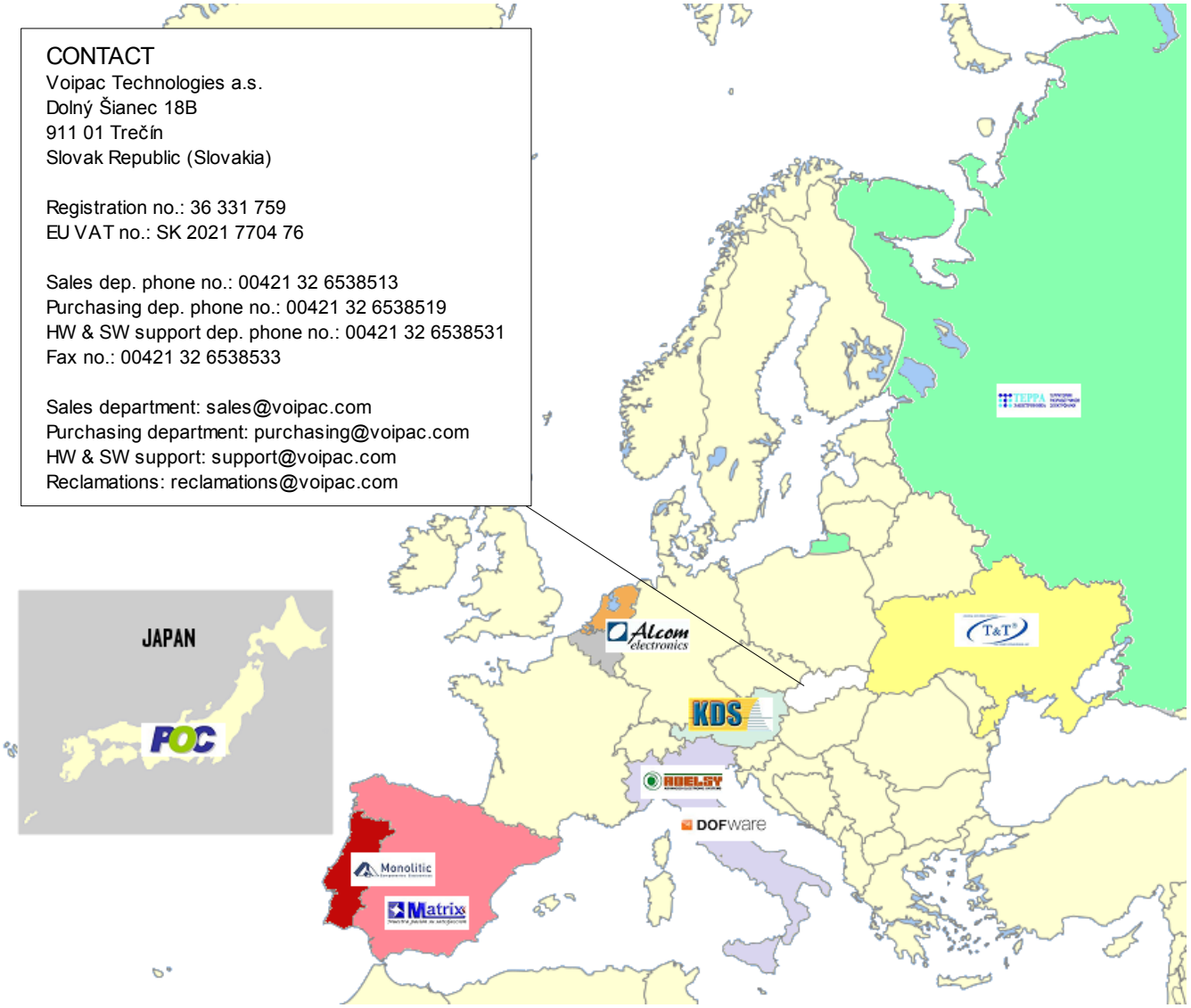
Alcom electronics nv/sa
Singel 3
2550 Kontich, Belgium
Phone: +32 3458 3033
Fax: +32 3458 3126
E-mail: info@alcom.be

Russian Federation

Terraelectronica Ltd.
Derbenevskaya 1, corps.1 entr. 23
115114 Moscow, Russia
Phone: 007 495 221 7803
Fax: 007 495 221 7802
E-mail: info@terraelectronica.ru

Japan

POSITIVE ONE CORPORATION
22F, Shibuya Mark City West
1-12-1, Shibuya-ku, Dougenzaka
Tokyo, Japan
Phone: +81-(0)3-5330-8648
Fax: +81-(0)3-4360-5301
E-mail: poc_sales@positive-one.com


CONTACT
Voipac Technologies a.s.
Dolný Šianec 18B
911 01 Trečín
Slovak Republic (Slovakia)
Registration no.: 36 331 759
EU VAT no.: SK 2021 7704 76
Sales dep. phone no.: 00421 32 6538513
Purchasing dep. phone no.: 00421 32 6538519
HW & SW support dep. phone no.: 00421 32 6538531
Fax no.: 00421 32 6538533
Sales department: sales@voipac.com
Purchasing department: purchasing@voipac.com
HW & SW support: support@voipac.com
Reclamations: reclamations@voipac.com
JAPAN
FOC
Alcom electronics
KDS
DOFware
Monolitic
Matrix
T&T

Warranty:

Voipac Technologies a.s. Does Not Bear Responsibility for the Following:

- Failure of a product resulting from misuse, accident, modification, unsuitable operating environment, or improper maintenance by user
- Unless otherwise agreed in written, a product does not include technical support and the customer may be able to purchase technical support under separate agreement
- Any technical or other support provided under warranty by Voipac Technologies a.s. such as assistance, set-up and installation is provided WITHOUT WARRANTY OF ANY KIND.

Disclaimer:

Voipac Technologies a.s. reserves the right to make changes, without notice, to any product, including circuits and/or software described or contained in this datasheet. Voipac Technologies a.s. assumes no responsibility or liability for the use of the described product(s), conveys no license or title under any patent, copyright, or mask work rights to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Trademark Acknowledgment:

Brand and product names are trademarks or registered trademarks of their respective owners.