

A faded, grayscale image of a DIMM module is centered in the background. The module is a rectangular printed circuit board with various components, including a large central chip and several smaller components. The text "Voipac PXA270 DIMM Module" and "Datasheet" is overlaid on the image in a large, bold, black font.

# Voipac PXA270 DIMM Module

## Datasheet

| Date               | Revision | Changes  |
|--------------------|----------|--|
| 20. September 2006 | 1.0      | Initial Release  |
| 17. April 2009     | 1.1      | Update   |
| 16. March 2011     |          | Added Support, Distributors and Ordering Information Chapter |

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## 1. Introduction

### 1.1 Hardware

Voipac PXA270 module is a SODIMM module based on the Intel XScale® PXA270 processor. It runs at up to 520 MHz and consumes as little as 800mW. The module delivers state of the art technology, targeting low power systems that still require high CPU performance.

Central component of the module is the PXA270 Intel XScale® processor supporting Intel® Wireless MMX™ technology. Low power requirements of the Voipac PXA270 module are achieved by using advanced power manager integrated circuit, which allows to fully control all power domains.

The Module is further equipped with SDRAM and FLASH memory chips, as well as an audio controller, 100Mbps ethernet controller full speed 12Mbps USB host and USB 2.0 OTG device functionality. Voipac PXA270 module can be supplied in a various processor and memory configurations.

Wireless Intel Speedstep® Technology, which adjusts the CPU core voltage dynamically according to the CPU load, four low-power modes, together with flexible power manager integrated circuit enable to achieve excellent MIPS/mW performance for the Voipac PXA270 module.

The entire 32 bit wide CPU bus together with available GPIO pins are available for custom extensions, such as special interfaces for high bandwidth applications.

### 1.2 Software

Since the PXA270 processor is ARM compatible various operating systems are available for the Voipac PXA270 module even by third parties. In case of unsupported operating system needed documentation for all hardware peripherals is freely available.

Voipac fully supports Linux operating system with drivers for all basic interfaces. Custom additional drivers for specific applications can be developed upon request.

| Operating system | Description                                       |
|------------------|---|
| Linux            | Linux 2.6 with drivers for most common interfaces |
| Windows CE       | Windows CE 6.0                                    |
| QNX              |   |

### 1.3 Features Summary

| Feature       | Description   |
|---------------|---|
| CPU           | PXA270@312-512MHz   |
| SDRAM         | 8-256MB 32bit   |
| FLASH         | 8-64MB 16bit  |
| STORAGE       | PCMCIA/CF interface 16bit, MMC/SD/SDIO interfaces               |
| LCD           | TFT/STN 18bit up to 1024x768                                    |
| AUDIO/TOUCH   | UCB1400 16bit up to 48kHz with resistive 4wire touch controller |
| VIDEO CAPTURE | CMOS/CCD image sensor interface                                 |
| ETHERNET      | DM9000E 10/100Mbps 32bit  |
| USB           | 2xUSB Host, 1xUSB 2.0 OTG device                                |
| OTHER I/O     | MSL (up to 416 Mbps), I2C, SPI, 3xRS232                         |

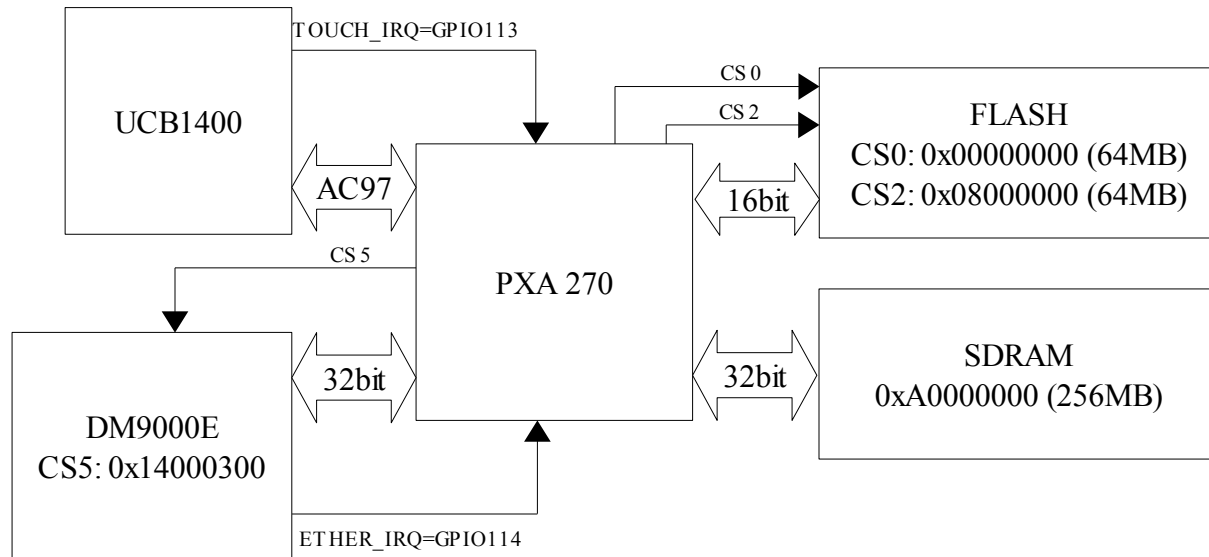
### 1.4 Reference Documents

For more detailed technical information about the Voipac PXA270 module components, please refer to the web resources and documents listed below.

| Component                           | Description   |
|-------------------------------------|---|
| Intel Xscale® PXA270 Processor      | <a href="http://voipac.com/fileDownload?fileName=Documents/pxa270dm.pdf">http://voipac.com/fileDownload?fileName=Documents/pxa270dm.pdf</a>                                   |
| Davicom DM9000E Ethernet Controller | <a href="http://www.davicom.com.tw/userfile/24247/DM9000-DS-F03-041906_1.pdf">http://www.davicom.com.tw/userfile/24247/DM9000-DS-F03-041906_1.pdf</a>                         |
| Philips UCB1400 Audio Controller    | <a href="http://www.nxp.com/pip/UCB1400BE.html">http://www.nxp.com/pip/UCB1400BE.html</a>   |
| Maxim MAX1587 Power Controller      | <a href="http://datasheets.maxim-ic.com/en/ds/MAX1586A-MAX1587C.pdf">http://datasheets.maxim-ic.com/en/ds/MAX1586A-MAX1587C.pdf</a>   |
| Intel StrataFlash® Embedded Memory  | <a href="http://www.mipsasoft.com/MS7/Hardware/FLASH/StrataFlash P30-T Data Sheet.pdf">http://www.mipsasoft.com/MS7/Hardware/FLASH/StrataFlash P30-T Data Sheet.pdf</a>       |
| SAMSUNG Mobile SDR SDRAM            | <a href="http://www.samsung.com/global/business/semiconductor/productList.do?fmly_id=136">http://www.samsung.com/global/business/semiconductor/productList.do?fmly_id=136</a> |

## 2. Functional Description

### 2.1 Block Diagram



The diagram shows internal interconnection of Voipac PXA270 module. Voipac PXA270 module features full 32 bit interfaces to on board SDRAM and ethernet controller. This results in maximum bandwidth for any data transfers.

Two chip select signals are used by on board 16bit FLASH and one for the ethernet controller thus are not available on SODIMM connector. Three additional chip selects can be used by external companion chips. The diagram further shows mapping of GPIO signals used as interrupt requests from ethernet and audio controller.

Since not all PXA270 interfaces have dedicated pins some functions could not be used simultaneously.

### 3. SODIMM Signal Description

This chapter describes the signals of the Voipac PXA270 module. Some pins have dedicated functionality, but most are highly multiplexed, so that the same pin can have up to 6 different roles and the same functionality is sometimes available alternatively on different pins. Each of these multiplexed pins is additionally also usable as a General Purpose Input/Output pin (GPIO). Additionally each GPIO pin can be used as interrupt source.

#### 3.1 IO Types Notation

| Signal | Description                 |
|--------|-----------------------------|
| IN     | Digital CMOS input          |
| OUT    | Digital CMOS output         |
| IO     | Digital CMOS input / output |
| AIN    | Analog input                |
| AOUT   | Analog output               |
| AIO    | Analog input / output       |
| PWR    | Power supply                |

#### 3.2 Pinout Description

| Pin# | Pin Name   | Type | Description                |
|------|------------|------|----------------------------|
| 1    | MIC_IN     | AIN  | Microphone Input           |
| 2    | AD3        | AIN  | AD Converter Input 3       |
| 3    | MIC_GND    | PWR  | Microphone Ground          |
| 4    | AD2        | AIN  | AD Converter Input 2       |
| 5    | LINEIN_L   | AIN  | Line Input (Left Channel)  |
| 6    | AD1        | AIN  | AD Converter Input 1       |
| 7    | LINEIN_R   | AIN  | Line Input (Right Channel) |
| 8    | AD0        | AIN  | AD Converter Input 0       |
| 9    | VSSA_AUDIO | PWR  | Audio Codec Ground         |

| Pin# | Pin Name       | Type | Description   |
|------|----------------|------|---|
| 10   | VDDA_AUDIO     | PWR  | Audio Codec Power supply (connect to 3.3V)  |
| 11   | VSSA_AUDIO     | PWR  | Audio Codec Ground  |
| 12   | VDDA_AUDIO     | PWR  | Audio Codec Power supply (connect to 3.3V)  |
| 13   | HEADPHONE_GND  | PWR  | Headphone Ground  |
| 14   | TSPX           | AIO  | 4wire Resistive Touch Panel (X Plus Terminal)   |
| 15   | HEADPHONE_L    | AOUT | Headphone Output (Left Channel)   |
| 16   | TSMX           | AIO  | 4wire Resistive Touch Panel (X Minus Terminal)  |
| 17   | HEADPHONE_R    | AOUT | Headphone Output (Right Channel)  |
| 18   | TSPY           | AIO  | 4wire Resistive Touch Panel (Y Plus Terminal)   |
| 19   | GPIO46/STD_RXD | IN   | Receive Pin for Standard UART   |
| 20   | TSMY           | AIO  | 4wire Resistive Touch Panel (Y Minus Terminal)  |
| 21   | GPIO47/STD_TXD | OUT  | Transmit Pin for Standard UART  |
| 22   | VDD_FAULT      | IN   | VDD Fault: This input signals that the main power source is going out of regulation. nVDD_FAULT causes the PXA27x processor to enter sleep mode or, if PMCR[VIDAE] is set, forces an imprecise-data abort, which cannot be masked. nVDD_FAULT is ignored after a wake-up event until the power supply timer completes (approximately 10 ms).                                      |
| 23   | GPIO40/FF_DTR  | OUT  | Full-Function UART Data-Terminal-Ready  |
| 24   | BATT_FAULT     | IN   | Main Battery Fault: This input signals that the main battery is low or removed. Assertion causes the PXA27x processor to enter sleep mode or, if PMCR[BIDAE] is set, forces an imprecise-data abort, which cannot be masked. The PXA27x processor does not recognize a wake-up event while this signal is asserted.   |
| 25   | GPIO100/FF_CTS | IN   | Full-Function UART Clear-to-Send  |
| 26   | nRESET_IN      | IN   | Reset: This active-low, level-sensitive input starts the processor from the reset vector at address 0. Assertion causes the current instruction to terminate abnormally and causes a reset. When nRESET is driven high, the processor starts execution from address 0. nRESET must remain low until the power supply is stable and the internal 13-MHz oscillator has stabilized. |
| 27   | GPIO27/FF_RTS  | OUT  | Full-Function UART Request-to-Send  |
| 28   | GPIO11         |      |   |
| 29   | GPIO33/FF_DSR  | IN   | Full-Function UART Data-Set-Ready   |
| 30   | GPIO16         |      |   |
| 31   | GPIO10/FF_DCD  | IN   | Full-Function UART Data-Carrier-Detect  |
| 32   | GPIO44/BT_CTS  | IN   | Bluetooth UART Clear-to-Send  |
| 33   | GPIO34/FF_RXD  | IN   | Full-Function UART Receive Data   |
| 34   | GPIO45/BT_RTS  | OUT  | Bluetooth UART Request-to-Send  |
| 35   | GPIO39/FF_TXD  | OUT  | Full-Function UART Transmit Data  |
| 36   | GPIO42/BT_RXD  | IN   | Bluetooth UART Receive Data   |
| 37   | GPIO38/FF_RI   | IN   | Full-Function UART Ring Indicator   |
| 38   | GPIO43/BT_TXD  | OUT  | Bluetooth UART Transmit Data  |
| 39   | GND            | PWR  | Ground  |
| 40   | +3V3           | PWR  | Main power supply (connect to 3.3V)   |
| 41   | GND            | PWR  | Ground  |
| 42   | +3V3           | PWR  | Main power supply (connect to 3.3V)   |
| 43   | GPIO0          |      |   |

| Pin# | Pin Name             | Type | Description  |
|------|----------------------|------|--|
| 44   | GPIO77/L_BIAS        | OUT  | LCD Bias Drive: AC bias that signals the LCD display module to switch the polarity of the power supplies to the row and column axis of the screen to counteract DC offset. In active (TFT) mode, it is used as the output enable to signal when data should be latched from the data pins using the pixel clock.   |
| 45   | GPIO1                |      |  |
| 46   | GPIO65/LDD07         | IO   | LCD Display Data 7   |
| 47   | GPIO32/MMCLK         | OUT  | MMC and SD/SDIO Card Bus Clock   |
| 48   | GPIO67/LDD09         | IO   | LCD Display Data 9   |
| 49   | GPIO109/MMDAT1       | IO   | MMC and SD/SDIO Data 1   |
| 50   | GPIO69/LDD11         | IO   | LCD Display Data 11  |
| 51   | GPIO110/MMDAT2/MMCS0 | IO   | SD/SDIO Data 2 or MMC Chip Select 0  |
| 52   | GPIO70/LDD12         | IO   | LCD Display Data 12  |
| 53   | GPIO111/MMDAT3/MMCS1 | IO   | SD/SDIO Data 3 or MMC Chip Select 1  |
| 54   | GPIO71/LDD13         | IO   | LCD Display Data 13  |
| 55   | GPIO19/L_CS          | OUT  | LCD Chip Select: Chip select signal for LCD panels with an internal frame buffer.  |
| 56   | GPIO76/L_PCLK_WR     | OUT  | LCD Pixel Clock: Pixel clock used by the LCD display module to clock the pixel data into the line shift register. In passive mode, the pixel clock toggles only when valid data is available on the data pins. In active mode, the pixel clock toggles continuously, and the AC bias pin is used as an output to signal when data is valid on the LCD data pins. This pin also functions as a write signal for LCD panels with an internal frame buffer. |
| 57   | GPIO86/LDD16         | IO   | LCD Display Data 16  |
| 58   | GPIO61/LDD03         | IO   | LCD Display Data 3   |
| 59   | GPIO12               |      |  |
| 60   | GPIO60/LDD02         | IO   | LCD Display Data 2   |
| 61   | GPIO87/LDD17         | IO   | LCD Display Data 17  |
| 62   | GPIO66/LDD08         | IO   | LCD Display Data 8   |
| 63   | GPIO14               |      |  |
| 64   | GPIO73/LDD15         | IO   | LCD Display Data 15  |
| 65   | GPIO106              |      |  |
| 66   | GPIO72/LDD14         | IO   | LCD Display Data 14  |
| 67   | GPIO17               |      |  |
| 68   | GPIO75/L_LCLK_A0     | OUT  | LCD Line Clock: Indicates the start of a new line. Also referred to as HSync (or horizontal synchronization) for active panels. For LCDs with an internal frame buffer, this signal indicates a command or data transaction.   |
| 69   | GPIO20               |      |  |
| 70   | GPIO59/LDD01         | IO   | LCD Display Data 1   |
| 71   | GPIO81               |      |  |
| 72   | GPIO63/LDD05         | IO   | LCD Display Data 5   |
| 73   | GPIO52               |      |  |
| 74   | GPIO68/LDD10         | IO   | LCD Display Data 10  |
| 75   | GPIO53               |      |  |
| 76   | GPIO58/LDD00         | IO   | LCD Display Data 0   |
| 77   | GPIO82               |      |  |
| 78   | GPIO62/LDD04         | IO   | LCD Display Data 4   |



| Pin# | Pin Name         | Type | Description   |
|------|------------------|------|---|
| 79   | GPIO83           |      |   |
| 80   | GPIO64/LDD06     | IO   | LCD Display Data 6  |
| 81   | GPIO84           |      |   |
| 82   | GPIO74/L_FCLK_RD | OUT  | LCD Frame Clock: Frame clock used by the LCD display module to signal the start of a new frame of pixels that resets the line pointers to the top of the screen. This pin is also the vertical synchronization signal for active (TFT) displays. This pin is the read signal during reads from a panel with an internal frame buffers.  |
| 83   | GND              | PWR  | Ground  |
| 84   | +3V3             | PWR  | Main power supply (connect to 3.3V)   |
| 85   | GPIO107          |      |   |
| 86   | GPIO24/SSPFRM    | IO   | Synchronous Serial Port 1 Frame: The serial frame sync can be configured as an output (master-mode) or an input (slave-mode).   |
| 87   | nRESET_OUT       | OUT  | Reset Out: Asserted when nRESET is asserted, it deasserts after nRESET is deasserted but before the first instruction fetch occurs. nRESET_OUT is asserted during power-on, hardware, watchdog, and sleep-exit resets. It is configurable for GPIO reset.   |
| 88   | GPIO23/SSPCLK    | IO   | Synchronous Serial Port 1 Clock: The serial bit-clock can be configured as an output (master-mode) or an input (slave-mode).  |
| 89   | nWE              | O    | Memory Write Enable: Connect to the write enables of SDRAM and static memory devices.   |
| 90   | GPIO26/SSPRXD    | IN   | Synchronous Serial Port 1 Receive Data: Serial data latched using the bit-clock.  |
| 91   | nOE              | O    | Memory Output Enable: Connect to the output enables of static memory devices to control data bus drivers.   |
| 92   | GPIO25/SSPTXD    | OUT  | Synchronous Serial Port 1 Transmit Data: Serial data driven out synchronously with the bit-clock.   |
| 93   | RDnWR            | OUT  | Read/Write: Indicates that the current transaction is a read (high) or a write (low)  |
| 94   | GPIO85/nPCE1     | OUT  | PC Card Enable 1: Selects a PC Card. nPCE1 enables the low byte lane.   |
| 95   | RDY(GPIO18)      | IN   | Variable Latency I/O Ready Pin: An external variable-latency I/O (VLIO) device asserts RDY when it is ready to transfer data.   |
| 96   | GPIO54/nPCE2     | OUT  | PC Card Enable 2: Selects a PC Card. nPCE2 enables the high byte lane.  |
| 97   | GPIO48/nPOE      | OUT  | PC Card Output Enable: Output enable for reads from PC Card memory and PC Card attribute space.   |
| 98   | GPIO55/nPREG     | OUT  | PC Card Register Select: Functions as address bit 26 to select register space (I/O or attribute) or memory space. Has the same timing as the address bus.   |
| 99   | nPWE(GPIO49)     | OUT  | PC Card Write Enable: Enables writes to PC Card memory and PC Card attribute space. Also serves as the write enable signal for variable-latency I/O.  |
| 100  | GPIO104/PSKTSEL  | OUT  | PC Card Socket Select: Used by external steering logic to route control, address, and data signals to one of the two PC Card sockets. Active-low output enable that can be used as nOE for the data transceivers. The signal has the same timing as the address bus.<br>In a single socket solution:<br>0 = Output enable selected<br>1 = Output enable not selected<br>In a dual socket solution, the socket select:<br>0 = Socket 0 selected<br>1 = Socket 1 selected |
| 101  | GPIO51/nPIOW     | OUT  | PC Card I/O Write: Asserted for writes to PC Card I/O space.  |
| 102  | GPIO56/nPWAIT    | IN   | PC Card Wait: Driven low by the PC Card to insert wait states, which extend transfers to and from the PXA27x processor.   |
| 103  | GPIO50/nPIOR     | OUT  | PC Card I/O Read: Asserted for reads from PC Card I/O space.  |

| Pin# | Pin Name              | Type | Description  |
|------|-----------------------|------|--|
| 104  | GPIO57/nIOIS16        | IN   | I/O Select 16: Input from the PC Card indicating that the data bus:<br>0 = Data bus is 8 bits wide<br>1 = Data bus is 16 bits wide   |
| 105  | GPIO15/nCS1           | OUT  | Static Chip Select 1: Physical Address 0x04000000<br>Static Chip Selects: Chip selects to static memory devices such as ROM and flash, individually programmable in the memory configuration registers.<br>nCS<5:0> can be used with variable-latency I/O devices.<br>nCS<3:0> can be used with synchronous flash. |
| 106  | GPIO80/nCS4           | OUT  | Static Chip Select 4: Physical Address 0x10000000  |
| 107  | GPIO79/nCS3           | OUT  | Static Chip Select 3: Physical Address 0x0C000000  |
| 108  | +3V3                  | PWR  | Main power supply (connect to 3.3V)  |
| 109  | GND                   | PWR  | Ground   |
| 110  | MA08                  | OUT  | MA[25:0] Memory Address Bus: Address for external memory accesses.   |
| 111  | MA00                  | OUT  |  |
| 112  | MA09                  | OUT  |  |
| 113  | MA01                  | OUT  |  |
| 114  | MA10                  | OUT  |  |
| 115  | MA02                  | OUT  |  |
| 116  | MA11                  | OUT  |  |
| 117  | MA03                  | OUT  |  |
| 118  | MA12                  | OUT  |  |
| 119  | MA04                  | OUT  |  |
| 120  | MA13                  | OUT  |  |
| 121  | MA05                  | OUT  |  |
| 122  | MA14                  | OUT  |  |
| 123  | MA06                  | OUT  |  |
| 124  | MA15                  | OUT  |  |
| 125  | MA07                  | OUT  |  |
| 126  | DQM0                  | OUT  | DQM Data Byte Mask Control 0: Corresponds to MD<7:0>.  |
| 127  | GPIO36/OTG_VBUS_EN    |      |  |
| 128  | DQM1                  | OUT  | DQM Data Byte Mask Control 1: Corresponds to MD<15:8>.   |
| 129  | GPIO89/USBH1_PEN      | OUT  | USB Host Power Enable: Controls power IC for USB host port.  |
| 130  | DQM2                  | OUT  | DQM Data Byte Mask Control 2: Corresponds to MD<23:16>.  |
| 131  | GPIO88/USBH1_OC       | IN   | USB Host Power Indicator: Over-current indicator from USB power IC for USB host port.  |
| 132  | DQM3                  | OUT  | DQM Data Byte Mask Control 3: Corresponds to MD<31:24>.  |
| 133  | GPIO37/OTG_VBUS_PULSE |      |  |
| 134  | MA25                  | OUT  |  |
| 135  | GPIO35/OTG_SRP_DETECT |      |  |
| 136  | MA24                  | OUT  |  |
| 137  | GPIO41/OTG_ID         |      |  |
| 138  | MA23                  | OUT  |  |
| 139  | USBH_P                | IO   | USB Host Positive Line: Differential signal connects to the USB host interface.  |

# Voipac PXA270 DIMM Module Datasheet



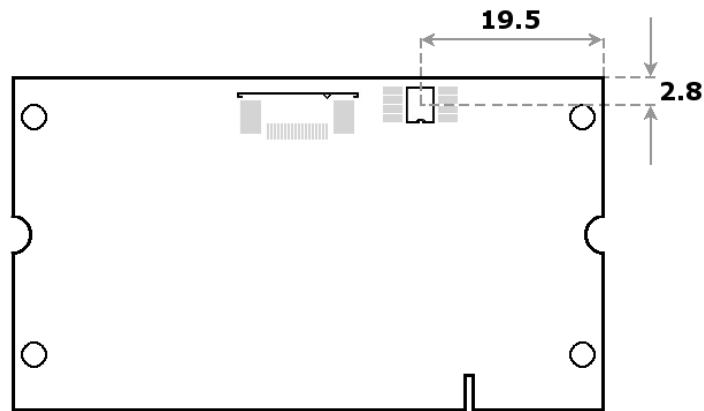
| Pin# | Pin Name | Type | Description   |
|------|----------|------|---|
| 140  | MA22     | OUT  |   |
| 141  | USBH_N   | IO   | USB Host Negative Line: Differential signal connects to the USB host interface.     |
| 142  | MA21     | OUT  |   |
| 143  | USBC_P   | IO   | USB Client Positive Line: Differential signal connects to the USB client interface. |
| 144  | MA20     | OUT  |   |
| 145  | USBC_N   | IO   | USB Client Negative Line: Differential signal connects to the USB client interface. |
| 146  | MA19     | OUT  |   |
| 147  | GND      | PWR  | Ground  |
| 148  | +3V3     | PWR  | Main power supply (connect to 3.3V)   |
| 149  | MD00     | IO   | MD[32:0] Memory Data Bus: Data bus to and from external memory devices.             |
| 150  | MD16     | IO   |   |
| 151  | MD01     | IO   |   |
| 152  | MD17     | IO   |   |
| 153  | MD02     | IO   |   |
| 154  | MD18     | IO   |   |
| 155  | MD03     | IO   |   |
| 156  | MD19     | IO   |   |
| 157  | MD04     | IO   |   |
| 158  | MD20     | IO   |   |
| 159  | MD05     | IO   |   |
| 160  | MD21     | IO   |   |
| 161  | MD06     | IO   |   |
| 162  | MD22     | IO   |   |
| 163  | MD07     | IO   |   |
| 164  | MD23     | IO   |   |
| 165  | MD08     | IO   |   |
| 166  | MD24     | IO   |   |
| 167  | MD09     | IO   |   |
| 168  | MD25     | IO   |   |
| 169  | MD10     | IO   |   |
| 170  | MD26     | IO   |   |
| 171  | MD11     | IO   |   |
| 172  | MD27     | IO   |   |
| 173  | MD12     | IO   |   |
| 174  | MD28     | IO   |   |
| 175  | MD13     | IO   |   |
| 176  | MD29     | IO   |   |
| 177  | MD14     | IO   |   |
| 178  | MD30     | IO   |   |
| 179  | MD15     | IO   |   |

| Pin# | Pin Name         | Type | Description                                  |
|------|------------------|------|--|
| 180  | MD31             | IO   |  |
| 181  | GND              | PWR  | Ground                                       |
| 182  | +3V3             | PWR  | Main power supply (connect to 3.3V)          |
| 183  | nETH_LINK_ACT    | OUT  | Ethernet Activity Indicator                  |
| 184  | MA18             | OUT  |  |
| 185  | nETH_SPEED100    | OUT  | Ethernet Speed Indicator                     |
| 186  | MA17             | OUT  |  |
| 187  | ETH_TXO-         | OUT  | Ethernet TX Differential Output (minus)      |
| 188  | MA16             | OUT  |  |
| 189  | ETH_TXO+         | OUT  | Ethernet TX Differential Output (plus)       |
| 190  | GPIO112/MMCMD    | IO   | MMC and SD/SDIO command and response tokens. |
| 191  | ETH_AGND         | PWR  | Ethernet Analog Ground                       |
| 192  | GPIO92/MMDAT0    | IO   | MMC and SD/SDIO Data 0                       |
| 193  | ETH_RXI-         | IN   | Ethernet RX Differential Input (minus)       |
| 194  | GPIO118/I2C_DATA | IO   | I2C Data: Serial data/address bus.           |
| 195  | ETH_RXI+         | IN   | Ethernet RX Differential Input (plus)        |
| 196  | GPIO117/I2C_CLK  | IO   | I2C Clock: Serial clock.                     |
| 197  | GND              | PWR  | Ground                                       |
| 198  | +3V3             | PWR  | Main power supply (connect to 3.3V)          |
| 199  | GND              | PWR  | Ground                                       |
| 200  | +3V3             | PWR  | Main power supply (connect to 3.3V)          |

## 4. Voipac PXA270 module Connectors

### 4.1 Physical Locations

Along with the main 200pin SODIMM connector the Voipac PXA270 module is equipped with one additional FCC connector (standardly not mounted) and pads for board-to-board pitch compression connector. The positions are shown in the figure below.



Dimensions are given in mm

### 4.3 JTAG

Connector: Molex 47041-0001 [www.molex.com](http://www.molex.com)

| Pin# | Pin Name | Type | Description                         |
|------|----------|------|-------------------------------------|
| 1    | +3V3     | PWR  | Supply power to power up JTAG logic |
| 2    | GND      | PWR  | Ground                              |
| 3    | TMS      | IN   | JTAG mode select                    |
| 4    | nTRST    | IN   | JTAG reset                          |
| 5    | TCK      | IN   | JTAG clock                          |
| 6    | TDO      | OUT  | JTAG Data output                    |
| 7    | TDI      | IN   | JTAG Data input                     |
| 8    | nSRST    | OUT  | System reset                        |

#### 4.4 Additional GPIOs (FCC1)

Connector: FCC 18 pins, 0.5mm pitch, bottom contact

| Pin# | Pin Name | Type | Description |
|------|----------|------|-------------|
| 1    | GPIO9    | IO   |             |
| 2    | GPIO13   | IO   |             |
| 3    | GPIO21   | IO   |             |
| 4    | GPIO22   | IO   |             |
| 5    | GPIO90   | IO   |             |
| 6    | GPIO91   | IO   |             |
| 7    | GPIO93   | IO   |             |
| 8    | GPIO94   | IO   |             |
| 9    | GPIO96   | IO   |             |
| 10   | GPIO97   | IO   |             |
| 11   | GPIO99   | IO   |             |
| 12   | GPIO101  | IO   |             |
| 13   | GPIO102  | IO   |             |
| 14   | GPIO103  | IO   |             |
| 15   | GPIO105  | IO   |             |
| 16   | GPIO108  | IO   |             |
| 17   | GPIO115  | IO   |             |
| 18   | GPIO116  | IO   |             |

## **5. Compatibility**

Voipac PXA270 modules can be used as a replacement for Toradex Colibri modules and after adjustments to GPIO pin mapping also for Keith & Koep's Trizeps III / IV family of modules. This chapter points out the differences for a smooth transition.

### **5.1 Toradex Colibri**

Voipac PXA270 module and Colibri share exactly the same pin mapping regarding all SODIMM pins. However, since Voipac PXA270 module implements four SDRAM banks some memory configurations will require two additional GPIO pins to be used as SDRAM chip selects and thus not available for customer designs.

The second FLASH bank also uses CS2 which is used by ethernet controller on Colibri module. By an assembly option it is possible to assign CS2 for ethernet controller too, while second FLASH bank is not being used. Additionally the ethernet controller has offset of 0x300 relative to used chip select physical base address.

### **5.1 Keith & Koep's Trizeps III / IV**

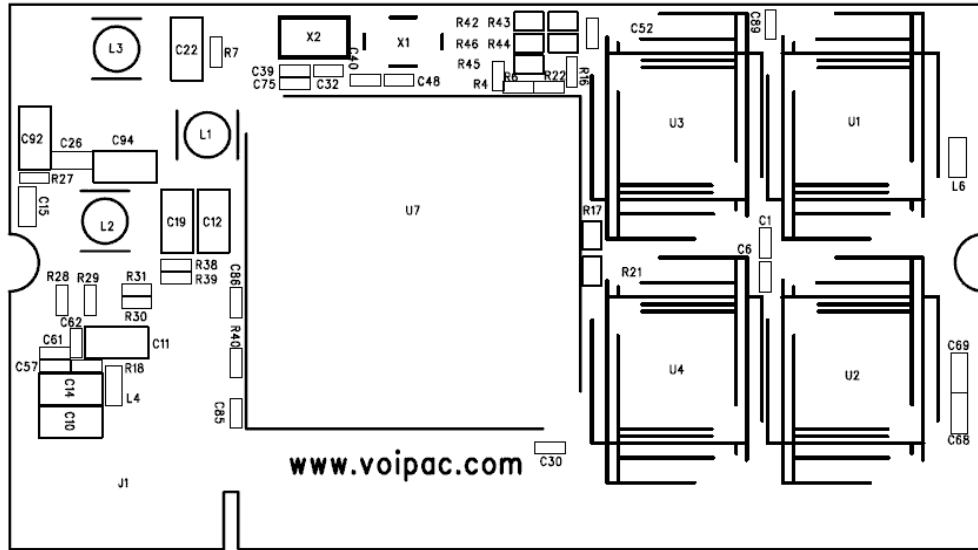
Voipac PXA270 module and Trizeps share a compatible pin mapping regarding all pins as GPIOs. However, the mapping GPIO to SODIMM pin is not identical. As long as Voipac PXA270 module pins are used only as GPIOs, the modules are hardware compatible.

Slight software adoptions are necessary in most projects to transition between Voipac PXA270 module and Trizeps III / IV to remap the GPIO pins.

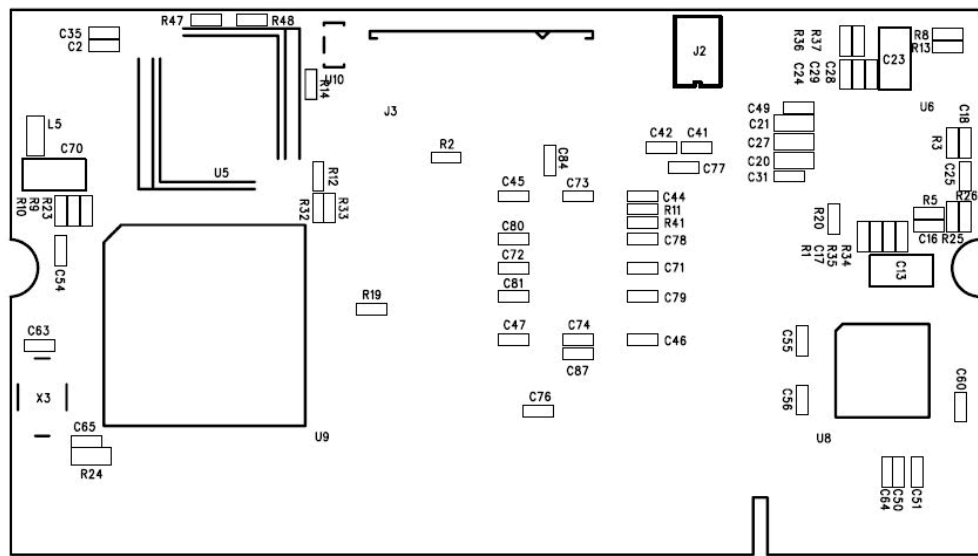




Top Layer



Bottom Layer



### 6.3 Sockets for the Voipac PXA270 module

The Voipac PXA270 module fits into a regular 2.5V DDR1 SODIMM memory socket

### 6.4 Temperature Range

| Symbol | Description                                  | Min | Type | Max | Unit |
|--------|--|-----|------|-----|------|
| T_AMB  | Operating temperature range                  | 0   |      | 70  | °C   |
| T_AMB  | Operating temperature range without ethernet | -25 |      | 85  | °C   |

### 6.5 RoHS and WEEE Compliance

All of the products designed and manufactured by Voipac Technologies are classified as Electrical and Electronic Equipment (EEE) under the Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment 2002/95/EC (RoHS). To comply with the RoHS directive, the restricted use of Lead (Pb), Mercury (Hg), Cadmium (Cd), Hexavalent Chromium (Cr 6+), Polybrominated Biphenyls (PBB) and Polybrominated Diphenyl Ethers (PBDE) must be ensured. Voipac Technologies guarantees that products ordered after July 1, 2006 are assembled in full compliance with the RoHS directive from the European Parliament and Counsel. The company procedures also complies with the Waste Electrical and Electronic Equipment Directive 2002/96/EC (WEEE) .

## 7. Support

All the relevant communication should be executed via e-mails preferably. Response time is up to 48 hours, except state holidays and weekends. Voipac Technologies working hours are: 8:00 - 17:00, Monday – Friday.

To claim warranty and RMA number assignment, please fill in this [protocol/problem description form](#) and send it to: [reclamations@voipac.com](mailto:reclamations@voipac.com).

Board warranty without the protocol/problem description will not be processed.

For more information, see our [General Terms and Conditions](#).

Besides the free-of-charge support, we provide support for your new designs when it comes to the special drivers for the peripherals not included in the Voipac development kits, design of your own base boards, prototyping, or even new products development, please contact: [support@voipac.com](mailto:support@voipac.com) for more info.

By [registering on Voipac's Internet Customer Details site](#), you will be granted to access the [Voipac Ticketing System](#), where you can post support request tickets and receive e-mail notifications upon any change of your ticket's status.

## 8. Distributors

### Austria

#### [KDS Handelsgesellschaft mBH](#)

Rienoesslgasse 22/11  
1040 Vienna, Austria  
Phone: 0043 1 7260408  
Fax: 0043 1 546804983  
E-mail: [office@kds.at](mailto:office@kds.at)

### Ukraine

#### [Technotrade Ltd](#)

Polupanova 10  
04114 Kiev, Ukraine  
Phone / Fax:  
0038 44 5024655 (-77)  
0038 44 2369055 (-57)  
E-mail: [voipac@tit.kiev.ua](mailto:voipac@tit.kiev.ua)

### Italy

#### [Adelsy srl](#)

via J. Lennon 6  
40057 Cadriano di Granarolo dell'Emilia, Italia  
Phone: 0039 51 763069  
Fax: 0039 51 763073  
E-mail: [Info@Adelsy.it](mailto:Info@Adelsy.it)

### Italy

#### [Dofware s.r.l.](#)

C.so IV Novembre, 7  
10036 Settimo Torinese, Italia  
Phone: 0039 011 569.24.45  
Fax: 0039 011 995.17.34  
E-mail: [Info@dofware.com](mailto:Info@dofware.com)

### Spain & Portugal

#### [Monolitic, s.a.](#)

Avda Vallcarca 78-80  
08023 Barcelona, Spain  
Phone: 0034 932859292  
Fax: 0034 932841193  
E-mail: [monolitic@monolitic.com](mailto:monolitic@monolitic.com)

### Spain & Portugal

#### [MATRIX ELECTRONICA](#)

C/Alejandro Sanchez, 109  
28019 Madrid, Spain  
Phone: +34 902 19 81 46  
Fax: +34 902 99 54 14  
E-mail: [matrix@matrix.es](mailto:matrix@matrix.es)

### The Netherlands

#### [Alcom Electronics bv](#)

Rivium 1e straat 52  
2909 LE Capelle ad IJssel  
Tel: +31.10.288.2500  
Fax: +31.10.288.2525  
E-mail: [info@alcom.nl](mailto:info@alcom.nl)

### Belgium

#### [Alcom electronics nv/sa](#)

[Singel 3](#)  
[2550 Kontich, Belgium](#)  
Phone: +32 3458 3033  
Fax: +32 3458 3126  
E-mail: [info@alcom.be](mailto:info@alcom.be)

**Russian Federation**

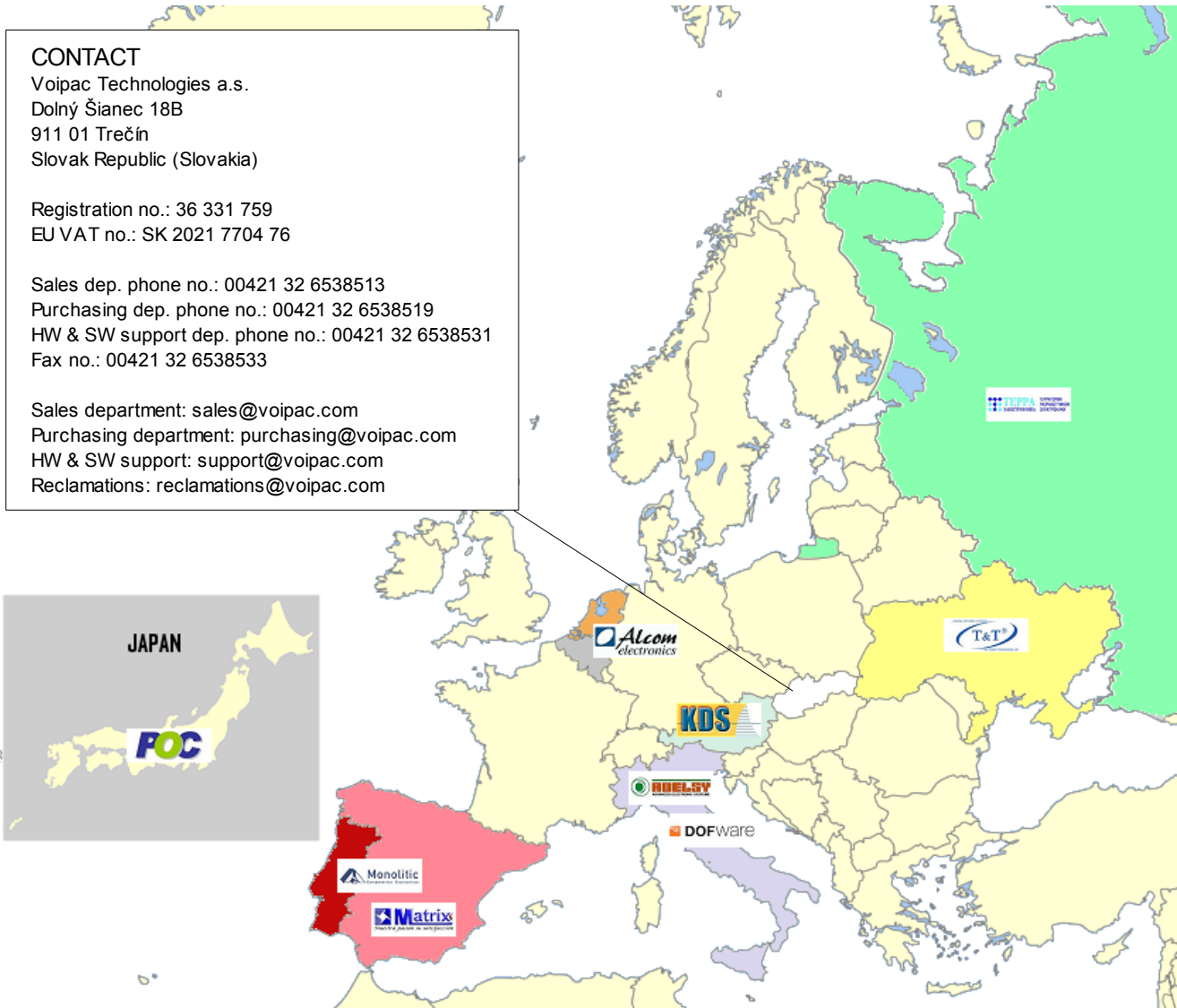
**Terraelectronica Ltd.**

Derbenevskaya 1, corps.1 entr. 23  
115114 Moscow, Russia  
Phone: 007 495 221 7803  
Fax: 007 495 221 7802  
E-mail: [info@terraelectronica.ru](mailto:info@terraelectronica.ru)

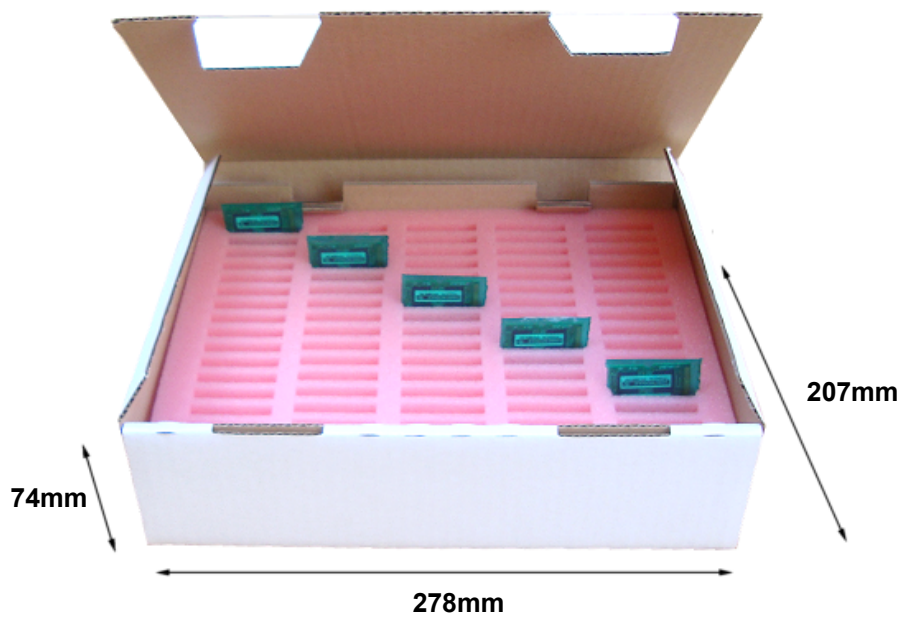
**Japan**

**POSITIVE ONE CORPORATION**

22F, Shibuya Mark City West  
1-12-1, Shibuya-ku, Dougenzaka  
Tokyo, Japan  
Phone: +81-(0)3-5330-8648  
Fax: +81-(0)3-4360-5301  
E-mail: [poc\\_sales@positive-one.com](mailto:poc_sales@positive-one.com)



## 9. Ordering Information



The standard box includes 75pcs of modules, each of them sealed in ESD plastic bag.

## Warranty:

### Voipac Technologies a.s. Does Not Bear Responsibility for the Following:

- Failure of a product resulting from misuse, accident, modification, unsuitable operating environment, or improper maintenance by user
- Unless otherwise agreed in written, a product does not include technical support and the customer may be able to purchase technical support under separate agreement
- Any technical or other support provided under warranty by Voipac Technologies a.s. such as assistance, set-up and installation is provided WITHOUT WARRANTY OF ANY KIND.

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