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DIMM PC

Development Kit User Manual
(preliminary version)

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1 Overview

Intel PXA255 DIMM PC board is intended for running embedded network applications. DIMM PC is designed mainly for the development of highly efficient Internet devices, and for network infrastructure applications, but it's use is on a large scale, cause it contains all of important interfaces.

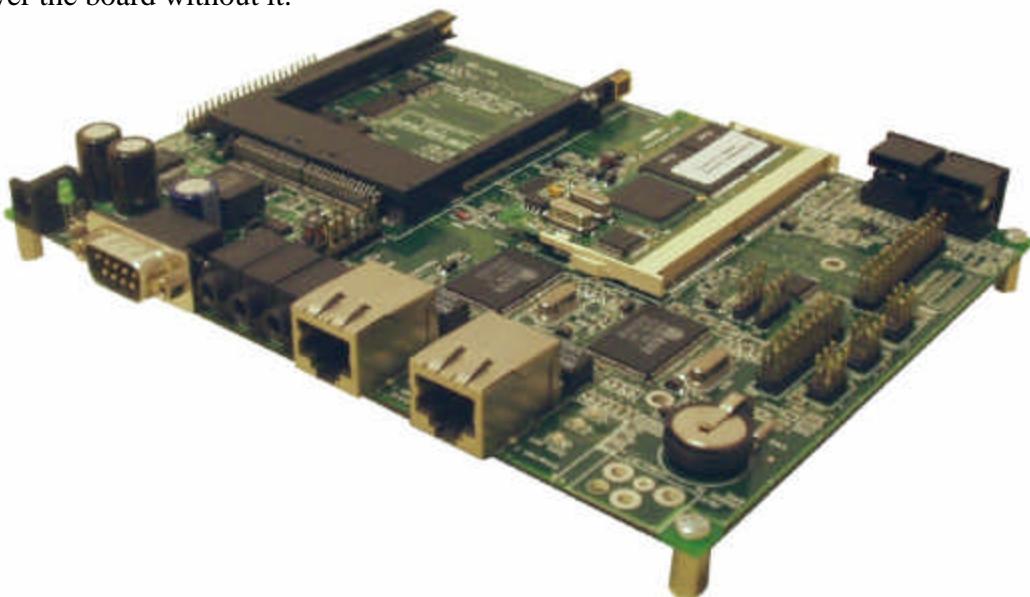
The DIMM PC is based on the new Intel XScale architecture. Intel XScale processor family increases efficiency and decreases processor power consumption. The Intel XScale micro architecture is based on the Intel Strong ARM technology. Intel Strong ARM and Intel XScale are compatible with the ARM architecture, which in turn guarantees the compatibility of software solutions.

DIMM PC is delivered in variety configurations, which may differ in processor frequency, SDRAM or FLASH size and amount of peripheries. CPU, SDRAM and FLASH memory is located on stand alone DIMM module, that means is easy to change processor frequency or memory size, without necessity to change main DIMM base board. If you need next extend FLASH storage space, plug Compact FLASH card in base board.

Furthermore, there are two network interfaces. The card contains two 3,3V PCMCIA slots and one 3,3V Compact FLASH connector. Two of them can be used at the same time. The board can be either powered by AC adapter or Power LAN system via power cord (outdoor application).

The board can be supplied in stylish case for indoor or outdoor application as well as with software for WLAN application, upon customer's request.

System is delivered with LINUX operating system. As the board communication interface serves RS232 connector. To work with on-board software easily and effectively, use terminal station. You may also use SSH network protocol. Your own applications can be stored in DIMM on-board FLASH memory or to the external Compact FLASH card. In the event that you are not interested to use software, we have developed, we will deliver the board without it.



1.1 Hardware specification

- DIMM module with XScale PXA 255
- 2 x 10/100Mb Ethernet
- 2 x PCMCIA slot, 1 x Compact Flash socket,
- 1 x IDE connector - in real time can work:
 - 2 x PCMCIA
 - 1 x PCMCIA + 1 x Compact Flash + 1 x IDE
- RS232 connector (terminal output)
- IR serial interface
- SPI interface
- UART serial connector (3.3-5V)
- JTAG connector
- RESET switch
- 6 - 30V power supply
- Power through LAN cable support
- Standard display interface with Touch screen
- Optional high color TFT display 640x480 STN display 320x240
- ATA2 interface for connecting HDD, CD-ROM, etc. (5V power suply)
- 2 x PS/2 - mouse and keyboard - controlled by programmable IO coprocessor
- Real Time Clock battery backup

Possible DIMM module configurations

- CPU XScale PXA255 200 - 400 MHz
- FLASH 8 - 32MB
- SDRAM 32 - 64MB
- AC97 audio (optional)

1.2 Software specification

- **OS Linux 2.4**
- File systems (ROMFS, JFFS2, EXT2, NFS, RAMFS)
- Terminal
- SSH,TFTP
- LINUX base utilities (Bash,Vi, ...)
- Network drivers
- DemoMP3player

2 Getting started

In this section is described how to connect your development kit and, how to begin with work.

Connecting the cables:

1. Connect serial cable to RS232 socket on board and to your computer.
2. Connect **Ethernet 1** (near to RS232 connector) cable to the board and to the switch/hub (if you want to connect directly to PC, you must use cross cable).
3. Insert DIMM module into DIMM socket. Be carefully.
4. On your PC run Hyper terminal or similar program with following parameters:
Baud rate – 38400
Data bits – 8
Parity – None
Stop bits - 1
Connection – COM1 or COM2, depends, where you connect serial cable.
5. Connect DC adapter into power jack. If you use other DC source, than supplied, ensure, that input voltage is in interval 9 - 28V DC. (outside pole of power jack is negative). If you are using display, you don't use supplied adapter, required current is about 1.5A.
6. When you power on the board, in terminal you can see following

```
pxa - HyperTerminal
Soubor Upravy Zobrazit Zavolat Windows Nastavení
ArmBoot>
ARMboot 1.2.0 by Voipac <www.voipac.com> (Sep 30 2003 - 19:19:07)
ARMboot code: a1000000 -> a10178d8
CPU: Intel KScale-PXA255 (ARM STE) revision A0
Clock: Mem=99.53MHz (~27), Run=199.07MHz (~2), Turbo=199.07MHz (~1.0,inactive)
DRAM Configuration:
Bank #0: a0000000 64 MB
Bank #1: a4000000 0 KB
Bank #2: a8000000 0 KB
Bank #3: ac000000 0 KB
Flash: 32 MB
*** Using default environment
Hit any key to stop autoboot: 0
Unknown command 'FIXME' - try 'help'
ArmBoot>
```

Figure 2-1 Terminal window

3 Hardware

3.1 Block Diagram

DIMM PC computer system consists of two basic elements:

- DIMM Base board
- DIMM processor modul

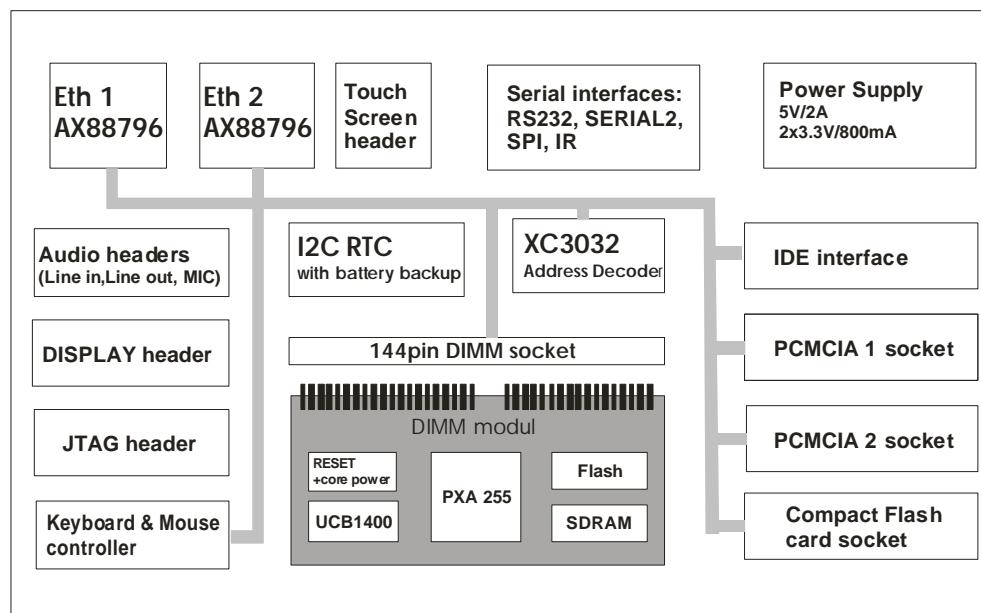


Figure 3-1 Block diagram of DIMM PC

3.2 Memory map

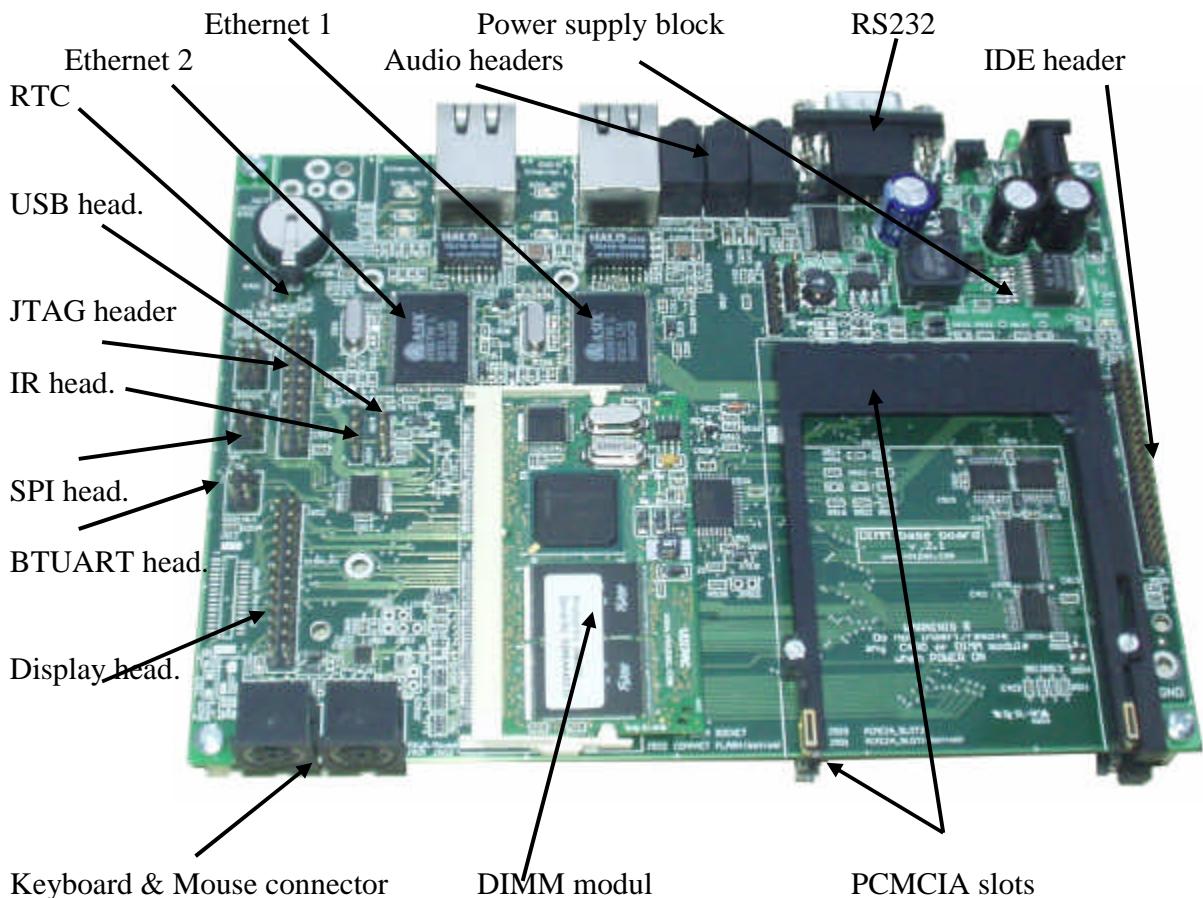
The board used standard address map with the following modification:

Pin	Description
CS0	(0-0x03FF.FFFF) flash memory
CS1	(0x0400.0000-0x07FF.FFFF) unused, used as GPIO pin
CS2	(0x0800.0000-0x0BFF.FFFF) Ethernet chip 1 (offset 0x400)
CS3	(0x0C00.0000-0x0FFF.FFFF) Ethernet chip 2 (offset 0x400) and PCMCIA status buffer (U502 – offset 0x0)
CS4	(0x1000.0000-0x13FF.FFFF) unused, used as GPIO pin
CS5	(0x1400.0000-0x17FF.FFFF) unused, used as GPIO pin
PCE1, PCE2 (PSKTSEL=0)	(0x2000.0000-0x2FFF.FFFF) PCMCIA 1 /CF, IDE
PCE1, PCE2 (PSKTSEL=1)	(0x3000.0000-0x3FFF.FFFF) PCMCIA 2

3.3 DIMM Base Board

3.3.1 Board Layout

All components (except PCMCIA2, CF card, touch screen and two display connectors) are located on top side of board.



3.3.2 Peripherals

3.3.2.1 JTAG

This interface is necessary by first time loading of the program into the FLASH memory. It is used together with JFLASHMM program (see in section 4.6.).

3.3.2.2 PXA255 serial ports

The PXA255 has three asynchronous serial ports (FFUART-SP0, BTUART-SERIAL2 and STUART-IR) and one synchronous serial port (SSPC).

The FFUART supports full handshaking. The maximum tested baud rate on this UART is 230.4 kbps. The BTUART supports RTS/CTS only and supports baud rates up to 921.6 kbps. STUART is tested at maximum baud rate 230.4kbps, but it does not support

modem control capability. STUART shares GPIO pins for transmit and receive data with the Fast Infrared Communication Port (FICP) –IR. It supports a variety of IrDA transceivers, operates at half-duplex and provides direct connection to commercially available Infrared Data Association (IrDA) compliant LED transceivers. FICP or Standard UART, only one of the ports can be used at a time.

The synchronous serial port (SSPC) supports three protocols: National Semiconductor's Microwire, Texas Instruments Synchronous Serial Protocol, and Motorola's Serial Peripheral Interface. SSPC supports serial bit rates from 7.2 KHz to 1.84 MHz and serial data formats may range from 4 to 16 bits in length.

Interface	Connector/Header
RS232-SP0	J605 – RS232
BTUART	J606 – SERIAL2
STURAT/IR	J604 – IR
SSPC	J607 – SPI

3.3.2.3 Ethernet controllers

There are two ASIX 100Mbit fast Ethernet chip AX88796. Each chip is equipped with three status LED's (active status, speed status, link status). **Only Ethernet 1 is default initialized in Armboot!**

3.3.2.4 PCMCIA sockets

PCMCIA sockets don't support plug and play! Don't plug/remove PCMCIA card if power is connected!

You can use 1 or 2 (depends, if Compact Flash or IDE device is used) 3.3V PCMCIA devices (like Wi-Fi, Ethernet, modem...). If some passive components are changed, there is possibility to use one 5V card.

PCMCIA status buffer is on address 0x0C00.0000. Use it for card properties reading.

Slot 1	Slot 2
4bit – BVD1	0bit – BVD1
5bit – BVD2	1bit – BVD2
6bit - Impact	2bit - Impact
7bit – Card detect	3bit – Card detect

3.3.2.5 Compact Flash slot

CF socket don't support plug and play! Don't plug/remove CF card if power is connected!

You can use it only for 3.3V compact flash card type I or II. OS Linux default support is for CF memory card.

3.3.2.6 HDD

If you need higher storage space, or more frequent number of write cycles, external 3.5 inch HDD can be connected to board. It can be any HDD designed for notebooks. The difference between these discs and standard 5.25" HDD is, that 3.5" drives need 5V supply only. Because it is standard IDE interface, there is possibility to connect two drives (one as a master, one as a slave) at time. You can use 2 HDD's or 1HDD and 1 CDROM (If you want to use CDROM, external 12V DC supply is required).

3.3.2.7 Display, touch-screen , backlight.

On the board is integrated digital video R-G-B interface for standard color and B/W displays. There are three displays connectors:

- Color TFT display SHARP LQ64D343 (J612)
- Color STN display HITACHI SX14Q004-ZZA (J615)
- Universal 2x13 pin header with all signals and I2C bus (J602)

Some displays are equipped with touch-screen. It can be connected to J611 or J616 (touch screen of HITACHI displays).

Board supports connection of inverters for many displays, 5V supply is condition (J603).

3.3.2.8 AC-97 stereo audio codec

In PXA255 implements a standard AC'97 Codec interface. A Philips UCB1400 AC'97 codec allows this interface to transmit and receive analog audio data. The UCB1400 is located at AC'97 input 0. UCB1400 also integrates a Headphone Output Amplifier, a Microphone Input Amplifier and Touch Screen controller.

3.3.2.9 USB

OPXA255 works as a USB client device also. To J614 you can connect USB master device (PC).

3.3.2.10 RTC

DS1339 RTC chip, 3V lithium battery backup and 32.768kHz clock are used. Device is connected on I2C bus, and is located on address 0xD0/0xD1 (first byte of I2C protocol). If you want to connect some external device via I2C bus, pins 20 and 22 of J602 are connected to this bus signals.

3.3.2.11 Keyboard and mouse controller

As a keyboard and mouse controller is used new Cygnal microcontroller C8051F30x. Main feature of chip are small dimension (3x3mm) and hardware support of I2C bus. If you do not want use mouse and keyboard and you need some other interface, there is possibility to upload own new firmware into Cygnal microcontroller.

3.3.2.12 Video Output (optional)

J613 is standard Cinch connector. It can be used only, if special video module (RGB to Composite video converter) is inserted to J602 connector.

3.3.3 Xilinx

XCR 3032 is used for address decoding. In following table is seen input and output signals. Equations and binary file for XCR 3032 are in source files of Development Kit CD.

Inputs		Outputs	
Name	Description	Name	Description
MA3	Data address bus	CE1_1	Chip Enable 1 for
MA4	Data address bus	CE2_1	Chip Enable 1 for
MA10	Data address bus	CE1_2	Chip Enable 1 for
MA16	Data address bus	CE2_2	Chip Enable 1 for
R/W	Signal Read/Write	CE1_3	Chip Enable 1 for
CS4	Address space CS4	CE2_3	Chip Enable 1 for
CS_E2	Address space CS_E2	CE1_4	Chip Enable 1 for
PCE1	CS1 signal for PCMCIA	CE2_4	Chip Enable 1 for
PCE2	CS2 signal for PCMCIA	CS_IDE	Selection of IDE communication
CD1_1	Card Inserted (PCMCIA slot 1)	CS_PCMCIA	Selection for PCMCIA status read
CD2_1	Card Inserted (PCMCIA slot 1)	PWAIT	WAIT signal (for PXA255)
CD1_2	Card Inserted (CF slot)	PIOIS16	8/16 bit transfer (for PXA255)
CD2_2	Card Inserted (CF slot)	P1_CD	Card inserted in Slot 1
CD1_3	Card Inserted (PCMCIA slot 2)	P2_CD	Card inserted in Slot 2
CD2_3	Card Inserted (PCMCIA slot 2)		
P1a_IOIS16	16 bit operation on PCMCIA1		
P1b_IOIS16	16 bit operation on CF slot		
P1c_IOIS16	16 bit operation on IDE interface		
P2_IOIS16	16 bit operation on PCMCIA2		
P1_WAIT	WAIT signal from PCMCIA1,CF,HDD		
P2_WAIT	WAIT signal from PCMCIA 2		
PSKTSEL	PCMCIA 1/2 select signal		

3.3.4 Connectors

J101 DIMM socket - 144pin DIMM socket for processor module

Detailed description in chapter 2.3.2

J201 LAN1 - RJ45 for ethernet1

Pin	Description	Pin	Description
1-2	TXD	4-5	Vcc - power on LAN
3-6	RXD	7-8	Vss – power on LAN

J301 LAN2 - RJ45 for ethernet2

Pin	Description	Pin	Description
1-2	TXD	3-6	RXD

J401 Power – power supply, DC 9-30V

Supply DC voltage 9-30V (connector: 5.5x2.1mm, centre positive)

J402 IDE – 44pin header for IDE interface (hdd, CDROM, etc...)

Pin	Description	Pin	Description
1	Reset/	2	Ground
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	Ground	20	KEY -removed
20	DMARQ	21	GND
23	IOW/	24	GND
25	IOR/	26	GND
27	IORDY/	28	CSEL
29	DMACK/	30	GND
31	IRQ	32	IOCS16/
33	A1	34	PDIAG/
35	A0	36	A2
37	CS1FX/	38	CS3FX/
39	DASP/	40	GND
41	+5V	42	+5V
43	GND	44	Reserved

J501 PCMCIA1 – PCMCIA1 socket (3.3V cards only)

Pin	Description	Pin	Description
1	GND	2	D3
3	D4	4	D5
5	D6	6	D7
7	CE1/	8	A10
9	OE/	10	A11
11	A9	12	A8
13	A13	14	A14
15	WE/	16	IREQ/
17	VCC	18	VPP1
19	A16	20	A15
21	A12	22	A7
23	A6	24	A5
25	A4	26	A3
27	A2	28	A1
29	A0	30	D0
31	D1	32	D2

33	IOIS16/	34	GND
35	GND	36	CD1/
37	D11	38	D12
39	D13	40	D14
41	D15	42	CE2/
43	VS1	44	IORD/
45	IOWR/	46	A17
47	A18	48	A19
49	A20	50	A21
51	VCC	52	VPP2
53	A22	54	A23
55	A24	56	A25
57	VS2	58	RESET
59	WAIT/	60	INPACK/
61	REG/	62	SPKR/
63	STSCHG/	64	D8
65	D9	66	D10
67	CD2/	68	GND

J502 COMPACT FLASH – Compact Flash card socket (3.3V cards only)

Pin	Description	Pin	Description
1	GND	2	D3
3	D4	4	D5
5	D6	6	D7
7	CE1/	8	A10
9	OE/	10	A9
11	A8	12	A7
13	VCC	14	A6
15	A5	16	A4
17	A3	18	A2
19	A1	20	A0
21	D0	22	D1
23	D2	24	IOIS16/
25	CD2/	26	CD1/
27	D11	28	D12
29	D13	30	D14
31	D15	32	CE2/
33	VS1/	34	IORD/
35	IOWR/	36	WE/
37	IRQ	38	VCC
39	CSEL/	40	VS2/
41	RESET	42	WAIT/
43	INPACK/	44	REG/
45	BVD2/SPKR	46	BVD1/STSCHG
47	D8	48	D9

49	D10	50	GND
----	-----	----	-----

J503 PCMCIA2 – PCMCIA2 socket (3.3V cards only)

Same as a PCMCIA1

J504 Xilinx JTAG – 6pin header for Xilinx programming

Pin	Description	Pin	Description
1	TMS	4	TCK
2	TDI	5	+3.3V
3	TDO	6	GND

J601 JTAG – JTAG/Debug port

Pin	Description	Pin	Description
1	VREF	2	+3.3V
3	nTRST	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	NC	12	GND
13	TDO	14	GND
15	nRESET	16	GND
17	NC	18	GND
19	NC	20	GND

J602 DISPLAY – Extended LCD display connector

Pin	Description	Pin	Description
1	H SYNC (Line CLK)	2	CLK (Dot Clock)
3	Red Data 1	4	V SYNC (Frame CLK)
5	Red Data 3	6	Red Data 2
7	Red Data 5 (MSB)	8	Red Data 4
9	Green Data 0 (LSB)	10	Green Data 1
11	Green Data 2	12	Green Data 3
13	Green Data 4	14	Green Data 5 (MSB)
15	Blue Data 1	16	Blue Data 2
17	Blue Data 3	18	Blue Data 4
19	Blue Data 5 (MSB)	20	SDA
21	ENAB (1=LCD ON)	22	SCL
23	+3.3V	24	+5V
25	GND	26	VIDEO_OUT

J603 Backlight – Backlight for LCD display

Pin	Description	Pin	Description
1	+5V	3	BCKL_ON – 1=Enable Backlight 0=Disable Backlight
2	GND	4	NC

J604 IR – Fast Infrared communication port (STUART/IR)

Pin	Description	Pin	Description
1	+3.3V	3	IR_TXD - transmit data
2	IR_MODE (GPIO 15 pin)	4	IR_RXD - received data
		5	GND

J605 RS232 – Standard serial asynchronous RS232 interface (V.28 voltage levels)

Pin	Description	Pin	Description
1	SP0 DCD	6	SP0 DSR
2	SP0 RXD	7	SP0 RTS
3	SP0 TXD	8	SP0 CTS
4	SP0 DTR	9	SP0 RI
5	GND		

J606 SERIAL2 – asynchronous serial port (BTUART), 5V I/O pins accept 5V,3.3V

Pin	Description	Pin	Description
1	SP1 CTS	2	SP1 TXD
3	SP1 RTS	4	+3.3V
5	SP1 RXD	6	GND

J607 SPI – Synchronous serial port (SSPC), 5V tolerant I/O pins accept 5V,3.3V

Pin	Description	Pin	Description
1	SSP FRM	2	SSP RXD
3	SSP CLK	4	+3.3V
5	SSP TXD	6	GND

J608 Line OUT – Stereo Line Out

Stereo jack for external headphones

J609 Line IN – Stereo Line In

Stereo jack for external audio source

J610 MIC – External Microphone

Input jack for external microphone

J611 TOUCH – Header for Touch Screen

Pin	Description	Pin	Description
1	TMSY	2	TMSX
3	TSPY	4	TSPX

J612 Display2 – Connector for display SHARP LQ64D343

Pin	Description	Pin	Description
1	GND	2	CLK (Dot Clock)
3	H SYNC (Line CLK)	4	V SYNC (Frame CLK)
5	GND	6	Red Data 0 (LSB) = GND
7	Red Data 1	8	Red Data 2

9	Red Data 3	10	Red Data 4
11	Red Data 5 (MSB)	12	GND
13	Green Data 0 (LSB)	14	Green Data 1
15	Green Data 2	16	Green Data 3
17	Green Data 4	18	Green Data 5 (MSB)
19	GND	20	Blue Data 0 (LSB) = GND
21	Blue Data 1	22	Blue Data 2
23	Blue Data 3	24	Blue Data 4
25	Blue Data 5 (MSB)	26	GND
27	ENAB (1=LCD ON)	28	+5V
29	+5V	30	NC
31	NC		

J613 Video_OUT – Composite video signal from extended Video modul for Base Board
Connected with J602-pin26

J614 USB – Header for USB

Pin	Description	Pin	Description
1	+3.3V	2	Data -
3	Data +	4	GND

J615 Display3 – Connector for display HIATCHI

Pin	Description	Pin	Description
1	VSYNC	2	H SYNC (Line CLK)
3	CLK (Dot CLK)	4	ENAB (1=LCD ON)
5	+3.3V	6	GND
7	V_CON	8	Data 0
9	Data 1	10	Data 2
11	Data 3	12	Data 4
13	Data 5	14	Data 6
15	Data 7	16	GND

J616 TOUCH – Connector for Touch Screen

Pin	Description	Pin	Description
1	TSMY	2	TSPX
3	TSPY	4	TSMX

3.3.5 Switch and led's

B101 - RESET switch - resets the system

D201 – Full duplex/Collision status Ethernet 1 device

D202 – Speed status Ethernet 1 device (10/100Mbit)

D203 – Link status Ethernet 1 device

D301 - Full duplex/Collision status Ethernet 2 device
 D302 - Speed status Ethernet 2 device (10/100Mbit)
 D303 - Link status Ethernet 2 device

D603 – power led

D801 – not used, usable, if new software is uploaded into Cygnal microcontroller

Jumpers

JP501 – CLOSE, if Xilinx is programmed
 JP802 – Cygnal RESET (CLOSE, OPEN if Cygnal controller is programmed)
 JP803 – not used, CLOSED, if Cygnal is programmed from PXA255
 J803 – not used, CLOSED, if Cygnal is programmed from PXA255

3.3.6 Power

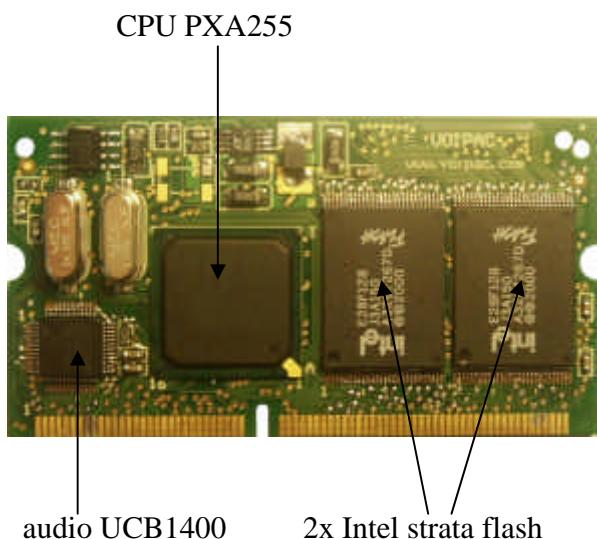
7. A standard 2.1mm DC jack is used to provide power the board. The center of jack is positive. It is recommended to power the board by stabilized source 9V-28V. If you are using display, you don't use supplied adapter, required current is about 1.5A (12V).

3.4 DIMM processor modul

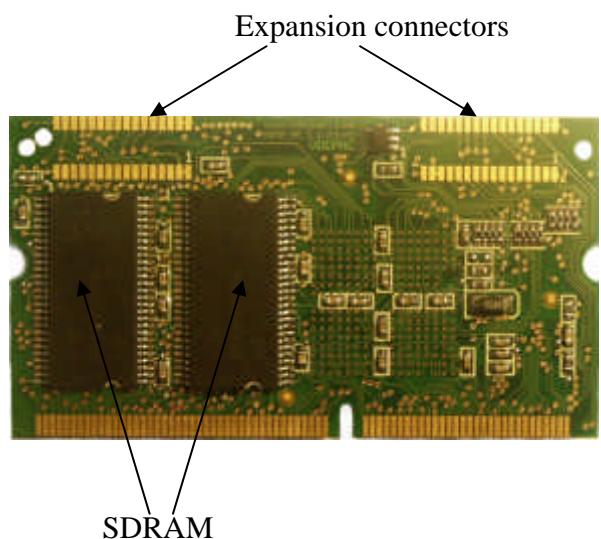
Don't plug/remove DIMM module if power is connected!

3.4.1 Board Layout

Top view



Bottom view



3.4.2 Connectors

Pin	Signal	Description
1	TSMY	Touch Screen, neg Y-connector (see UCB 1400)
2	TSMX	Touch Screen, neg X-connector (see UCB 1400)
3	TSPY	Touch Screen, pos Y-connector (see UCB 1400)
4	TSPX	Touch Screen, pos X-connector (see UCB 1400)
5	MICP	Microfon Input (see UCB 1400)
6	FF_RI	Full Function UART Ring Indicator (TTL-Level)
7	MICGND	Microfon GND – Signal (see UCB 1400)
8	LINE_IN_R	Line_In – right channel (see UCB 1400)
9	LINE_OUT_R	Line_Out – right channel (see UCB 1400)
10	LINE_IN_L	Line_In – left channel (see UCB 1400)
11	VREFDRV	reference voltage for head phone driver (see UCB 1400)
12	LINE_OUT_L	Line_Out – left channel (see UCB 1400)
13	AD3	Analog Input 3 (see UCB 1400)
14	AD2	Analog Input 2 (see UCB 1400)
15	AD1	Analog Input 1 (see UCB 1400)
16	AD0	Analog Input 0 (see UCB 1400)
17	AGND	Analog GND
18	GND	GND
19	TMS	JTAG Test Mode Select
20	TCK	JTAG Test Clock
21	TRST#	JTAG Test Reset
22	TDO	JTAG Test Data Out
23	RESET_INPUT	# Reset Input
24	TDI JTAG	Test Data In
25	RESET_OUT#	Reset Output
26	L_BIAS / GPIO77	LCD bias drive
27	BT_RxD / GPIO42	Bluetooth UART Receive Pin (3,3V-Level)
28	BATT_FAULT	Battery Fault, switches processor into sleepmode
29	BT_TxD / GPIO43	Bluetooth UART Transmit Pin (3,3V-Level)
30	IR_RXD / GPIO46	IrDA Receive Pin (3,3V- Level)
31	FF_RxD / GPIO34	Full Function UART Peceive Pin (3,3V-Level)
32	IR_TxD / GPIO47	IrDA Transmit Pin (3,3V-Level)
33	FF_TxD / GPIO39	Full Function UART Transmit Pin (3,3V-Level)
34	USB_N	USB-Port neg. Pin (3,3V-Level)
35	+3,3V_A	analogpower supply for audio
36	+3,3V	power supply
37	SDA	I2C data signal
38	USB_P	USB-Port pos. Pin (3,3V-Level)
39	SSP_TxD / GPIO25	Synchronous Serial Port Transmit Pin
40	SCL	I2C Clock Signal
41	SSP_CLK / GPIO23	Synchronous Serial Port Clock Pin
42	SSP_FRM / GPIO25	Synchronous Serial Port Frame Pin
43	DREQ0 / GPIO20	DMA Request Channel 0
44	SSP_RxD / GPIO26	Synchronous Serial Port Receive Pin

45	FF_DCD / GPIO36	Full Function UART Carrier Detect Pin (3,3V Level)
46	DREQ1 / GPIO19	DMA Request Channel 1
47	FF_DTR / GPIO40	Full Function UART Data Term. Rdy. Pin (3,3V-Level)
48	FF_DSR / GPIO37	Full Function UART Data Set Rdy. Pin (3,3V-Level)
49	FF_RTS / GPIO41	Full Function UART Rdy. To Send Pin (3,3V-Level)
50	FF_CTS / GPIO35	Full Function UART Clear To Send Pin (3,3V-Level)
51	BT_RTS / GPIO45	Bluetooth UART Ready To Send Pin (3,3V-Level)
52	BT_CTS / GPIO44	Bluetooth UART Clear To Send Pin (3,3V-Level)
53	GPIO10 General	Purpose I/O-Pin
54	GPIO11 General	Purpose I/O-Pin
55	LDD14 / GPIO72	LCD interface data bus
56	LDD15 / GPIO73	LCD interface data bus
57	LDD12 / GPIO70	LCD interface data bus
58	LDD13 / GPIO71	LCD interface data bus
59	LDD10 / GPIO68	LCD interface data bus
60	LDD11 / GPIO69	LCD interface data bus
61	LDD8 / GPIO66	LCD interface data bus
62	LDD9 / GPIO67	LCD interface data bus
63	GPIO0	General Purpose I/O-Pin
64	GPIO1	General Purpose I/O-Pin
65	GND	Ground
66	GND	Ground
67	L_FCLK / GPIO74	LCD Interface Frame Clock
68	L_LCLK / GPIO75	LCD Interface Line Clock
69	L_PCLK / GPIO76	LCD Interface Pixel Clock
70	LDD6 / GPIO64	LCD interface data bus
71	LDD7 / GPIO65	LCD interface data bus
72	LDD4 / GPIO62	LCD interface data bus
73	LDD5 / GPIO63	LCD interface data bus
74	LDD2 / GPIO60	LCD interface data bus
75	LDD3 / GPIO61	LCD interface data bus
76	LDD0 / GPIO58	LCD interface data bus
77	LDD1 / GPIO59	LCD interface data bus
78	GND	Ground
79	PWE# / GPIO49	PCMCIA Interface Write Enable
80	POE# / GPIO48	PCMCIA Interface Output Enable
81	PIOW# / GPIO51	PCMCIA Interface I/O Write
82	PIOR# / GPIO50	PCMCIA Interface I/O Read
83	PWAIT# / GPIO56	PCMCIA Interface Wait
84	PIOIS16# / GPIO57	PCMCIA Interface I/O select 16 Bit
85	PREG# / GPIO55	PCMCIA Interface Register Select
86	PSKTSEL / GPIO54	PCMCIA Interface Socket Select
87	PCE1# / GPIO52	PCMCIA Interface Low Byte Enable
88	PCE2# / GPIO53	PCMCIA Interface High Byte Enable
89	+3,3V	power supply
90	+3,3V	power supply

91	D14	memory data bus
92	D15	memory data bus
93	D12	memory data bus
94	D13	memory data bus
95	D10	memory data bus
96	D11	memory data bus
97	D8	memory data bus
98	D9	memory data bus
99	D6	memory data bus
100	D7	memory data bus
101	D4	memory data bus
102	D5	memory data bus
103	D2	memory data bus
104	D3	memory data bus
105	D0	memory data bus
106	D1	memory data bus
107	GND	Ground
108	GND	Ground
109	RDY / GPIO18	Ready Pin (Wait)
110	WE#	Memory Write Enable
111	RD/WR#	Read not Write
112	OE#	Memory Output Enable
113	GND	Ground
114	CS5# / GPIO33	Chip Select
115	CS4# / GPIO80	Chip Select
116	CS3# / GPIO79	Chip Select
117	CS2# / GPIO78	Chip Select
118	CS1# / GPIO15	Chip Select
119	A25	Memory address bus
120	A24	Memory address bus
121	A23	Memory address bus
122	A22	Memory address bus
123	A21	Memory address bus
124	A20	Memory address bus
125	A19	Memory address bus
126	A18	Memory address bus
127	A17	Memory address bus
128	A16	Memory address bus
129	A15	Memory address bus
130	A14	Memory address bus
131	A13	Memory address bus
132	A12	Memory address bus
133	A11	Memory address bus
134	A10	Memory address bus
135	A9	Memory address bus
136	A8	Memory address bus

137	A7	Memory address bus
138	A6	Memory address bus
139	A5	Memory address bus
140	A4	Memory address bus
141	A3	Memory address bus
142	A2	Memory address bus
143	A1	Memory address bus
144	A0	Memory address bus

3.4.3 Description of on-board devices

CPU

Intel PXA255 is used. Possible frequency is 200, 300 or 400MHz.

SDRAM

Modul uses two 256 or 512 Mbit SDRAM devices organized as one 32-Bit Bank (16Mx32bit or 8Mx32bit). They support 100MHz operation.

FLASH memory

4, 8 or 16MB Intel Strata Flash memory chips are used.

Used chips	Total capacity
E28F320-J3 (4MByte)	8MByte (2Mx32bit)
E28F640-J3 (8MbByte)	16MByte (4Mx32bit)
E28F128-J3 (16MByte)	32MByte (8Mx32bit)

4 Software & Development Tools

System is supplied with following software configuration:

Bootloader: Armboot ver. 1.2.0 (ethernet system loading support)

Linux OS: Debian Linux ver. 2.4.19

4.1 *DIMM module software preparation*

4.1.1 JTAG cable

Is needed for first Armboot flashing.

4.1.2 Bootloader Burning

Boards are delivered with bootloader. If you need change or update this software use JTAG or Ethernet.

For first board flashing use JTAG cable. You can us it when

4.1.3 Armboot

*** Under construction ***

4.1.4 Network Flashing (kernel and file system)

*** Under construction ***

4.2 OS linux preparation**4.2.1 TFTP server**

*** Under construction ***

4.2.2 Cross Compiler Installation

*** Under construction ***

4.2.3 Preparation of OS linux kernel source codes

*** Under construction ***

4.2.4 OS linux kernel preparation

*** Under construction ***

4.2.5 File system preparation

*** Under construction ***

4.2.6 Starting of OS

*** Under construction ***

4.3 Board customization

4.3.1 Xilinx

4.3.2 Microcontroller Cygnal

4.3.3 Display

4.3.4 External devices mapping into processor memory space

4.4 Peripherals using

4.4.1 Serial ports

4.4.2 Ethernet

4.4.3 PCMCIA

4.4.4 CF

4.4.5 HDD

4.4.6 Display, Touch-screen, and Backlight

4.4.7 Audio

4.4.8 RTC

4.4.9 Keyboard and mouse

4.5 Connecting to the board

We need two connections: via serial port and Ethernet network. Serial port we use as console and network we use for downloading file to the board memory. Serial console use direct serial cable, connect it to RS232 on PXA Board and computer. Start terminal on computer (on Debian minicom, gtkterm) with configuration:

- 38400 baud rate
- 8 data bits
- None Parity
- 1 Stop-Bit
- None Flow Control

For ethernet network use

- crossover cable to PC or
- direct cable to hub

Boards are delivered with bootloader. If you need change or update this software use JTAG or Ethernet.

For first board flashing use JTAG cable. You can us it when

4.6 Flashing kernel and rootfs via Ethernet network

Armboot screeen

```
ARMboot 1.0.2 (Jun 9 2003 - 12:53:59)

ARMboot code: a3000000 -> a301751c
CPU: Intel XScale-PXA250 (ARM 5TE) revision B2
Clock: Mem=99.53MHz (*27), Run=199.07MHz (*2), Turbo=199.07MHz (*1.0,inactive)
DRAM Configuration:
Bank #0: a0000000 32 MB
Bank #1: a4000000 0 KB
Bank #2: a8000000 0 KB
Bank #3: ac000000 0 KB
Flash: 8 MB
*** Using default environment
Hit any key to stop autoboot: 0
Unknown command 'FIXME' - try 'help'
ArmBoot>
```

Firstly we set IP address board and tftp server. Default address is 192.168.1.160 for board and 192.168.1.76 for tftp server. We can change it, but it depends on your network environment.

```
ArmBoot> setenv ipaddr 192.168.1.100
ArmBoot> setenv serverip 192.168.1.111
ArmBoot> saveenv
Un-Protected 1 sector
Saving Environment to Flash... done
Protected 1 sector
ArmBoot>
```

Then we erase flash for kernel (bank 1, sector 1 to 3).

```
ArmBoot> erase 1:1-3
Erase Flash Sectors 1-3 in Bank # 1:
Erasing sector 1 ... ok
Erasing sector 2 ... ok
Erasing sector 3 ... ok
Done
ArmBoot>
```

Now we can download kernel to the memory and then copy to the flash

(0xa0000000 is in RAM, 0x40000 is flash and 0x30000 is length). Length is in long (4bytes), because the bus width is 32 bit.

```
ArmBoot> tftpboot 0xa0000000 pxa/zImage
ARP broadcast 1
eth addr: 00:50:04:e0:31:f3
TFTP from server 192.168.1.111; our IP address is 192.168.1.100
Filename 'pxa/zImage'.
Load address: 0xa0300000
Loading: #####
Done
CHAPTER 4. BOARD USING 22
Bytes transferred = 654788 (9fdc4 hex)
ArmBoot>
```

Now we can copy downloaded file into flash

```
ArmBoot> cp.b 0xa0300000 0x40000 0x30000
Copy to Flash... 100% done.
ArmBoot>
```

We erase flash for rootfs (bank 1, sector 4 to 31),

```
ArmBoot> erase 1:4-31
Erase Flash Sectors 4-31 in Bank # 1:
Erasing sector 4 ... ok.
...
Erasing sector 31 ... ok.
Done
ArmBoot>
```

Now download /rootfs to the memory and copy to the flash.

```
ArmBoot> tftpboot 0xa0000000 pxa/crfs-root.bin
ARP broadcast 1
eth addr: 00:50:04:e0:31:f3
TFTP from server 192.168.1.111; our IP address is 192.168.1.100
Filename 'voipac2/crfs-root.bin'.
Load address: 0xa0000000
Loading: #####
Done
Bytes transferred = 4075520 (3e3000 hex)
```

```
ArmBoot>
```

And can copy downloaded file into flash

```
ArmBoot> cp 0xa0000000 0x10000 0x100000
Copy to Flash... 100% done.
ArmBoot>
```

Now we can start kernel by command go 0x40000. The default password for user root is root. You can connect via serial port again and now via ethernet network ssh 192.168.1.100 too.

5 Production and Distribution

Production:

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